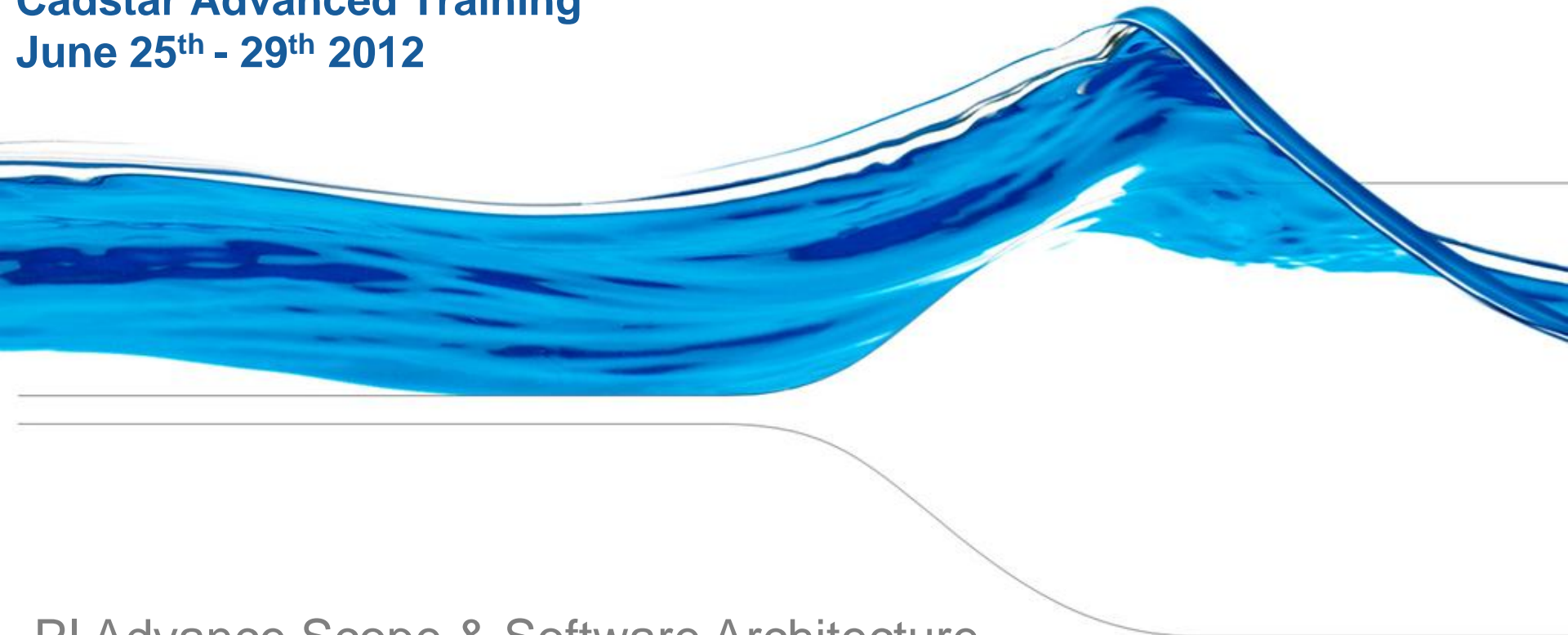


# Cadstar Advanced Training

## June 25<sup>th</sup> - 29<sup>th</sup> 2012



## PI Advance Scope & Software Architecture

Ralf Brüning

Product Manager High Speed Design Solutions/ Senior  
Partner

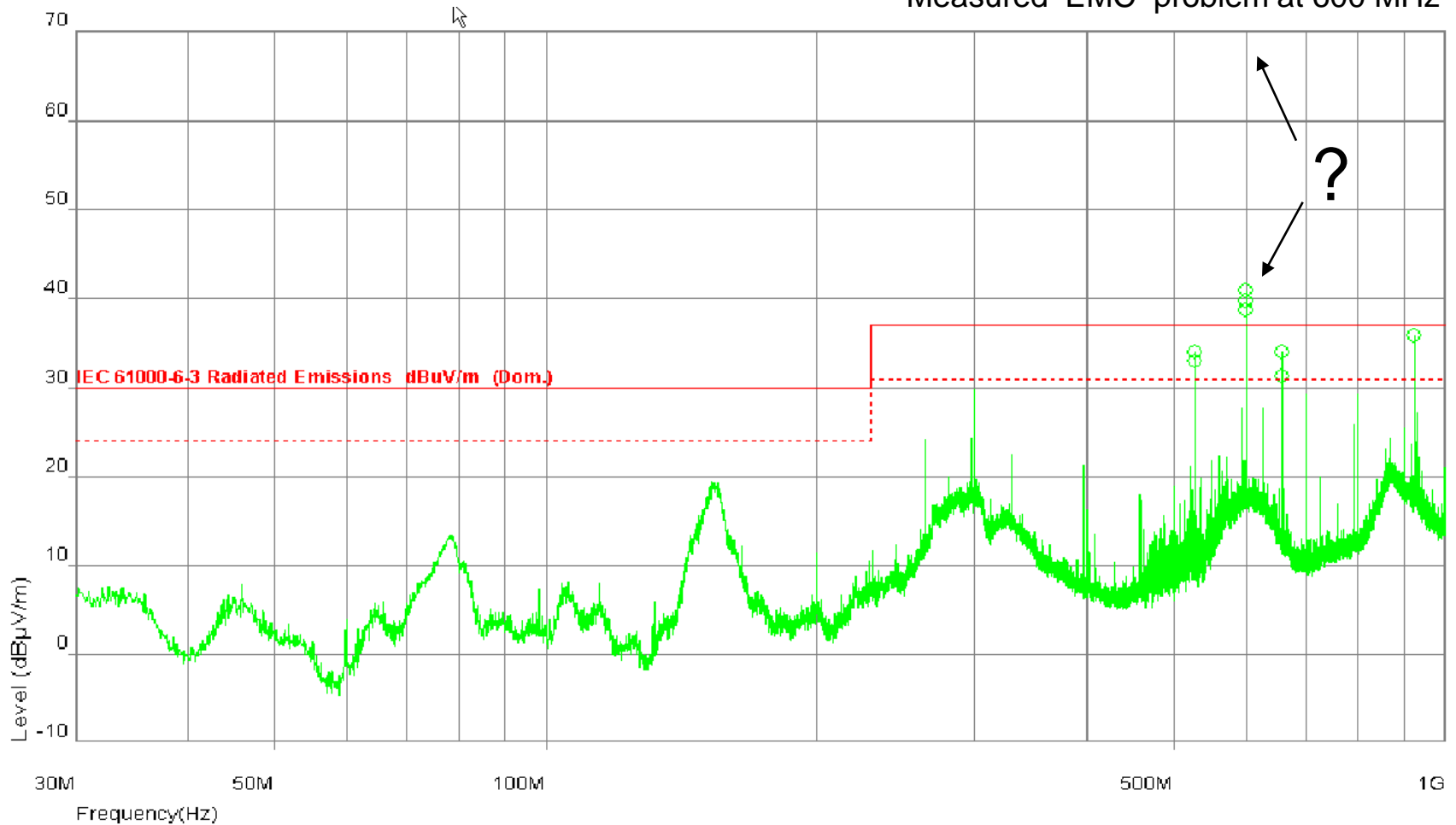
Zuken EMC Technology Center Paderborn





## EMC measurement result:

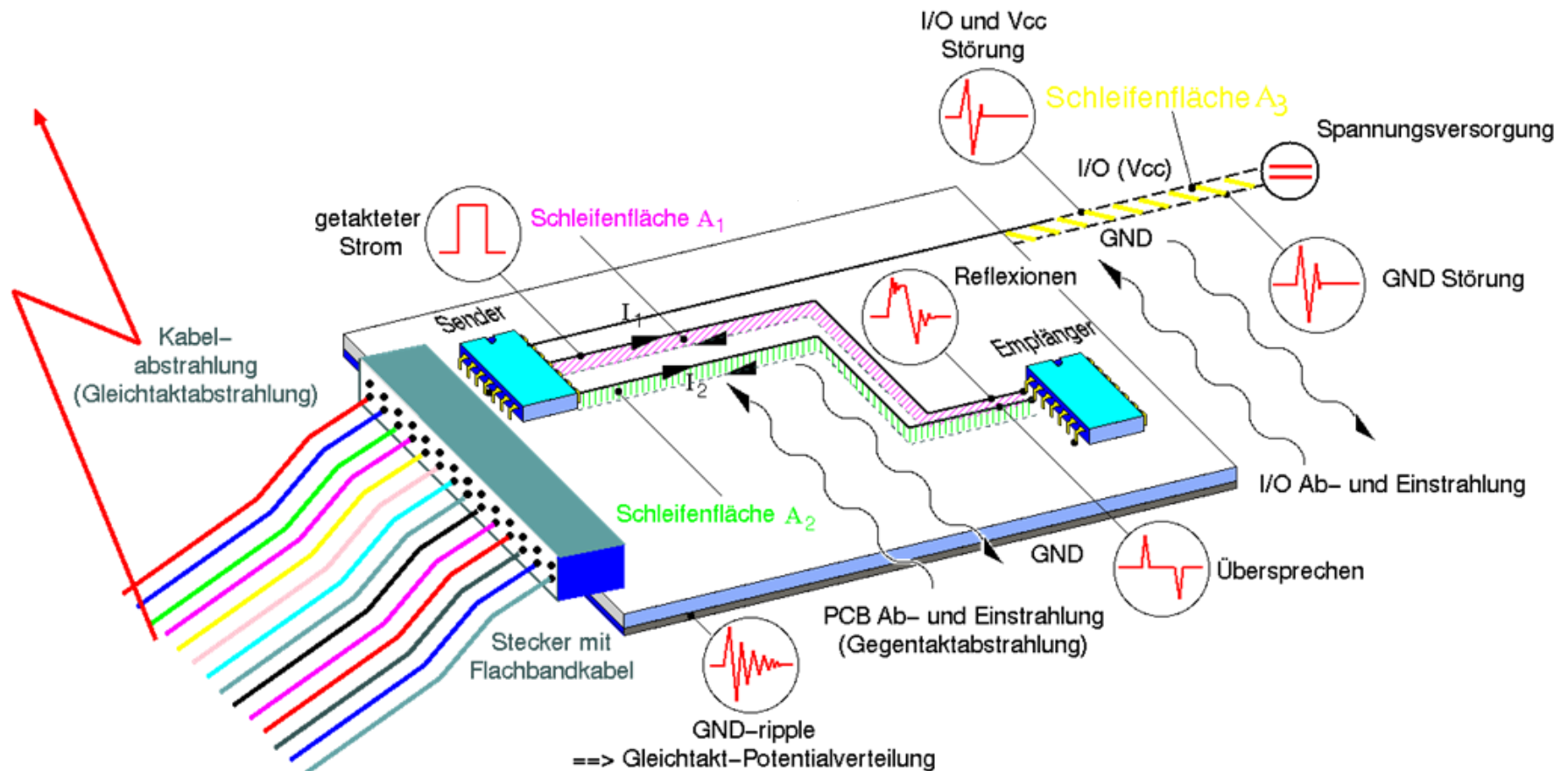
Measured EMC problem at 600 MHz





# EMC-Mechanisms on PCBs

## The “EMC-Nightmare” of a PCB





# Some Basics #0

## Decibel ? Why dB ? What is that ?

Decibel notation will characterize the relation or proportion between 2 quantities rather than giving just single value

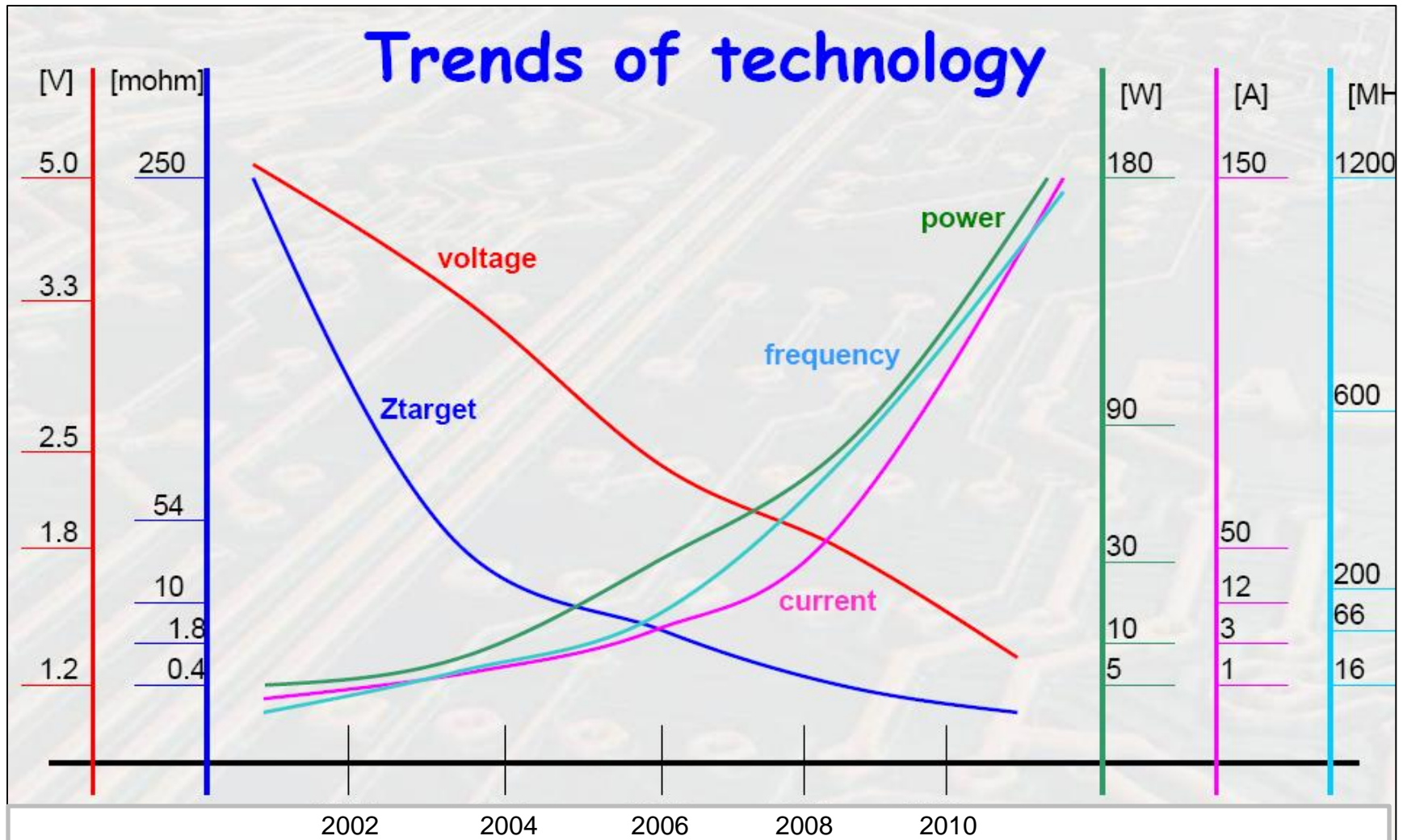
$$r = 10 \cdot \log_{10} \left( \frac{P_1}{P_2} \right) = 10 \cdot \log_{10} \left( \frac{U_1^2 / R}{U_2^2 / R} \right) = 20 \cdot \log_{10} \left( \frac{U_1}{U_2} \right)$$

$$dB\mu V \equiv 20 \cdot \log_{10} \left( \frac{U \text{ in V}}{1\mu V} \right)$$

Ratio	dB
1000000	120
100000	100
10000	80
1000	60
100	40
10	20
5	13,98
3	9,54
2	6,02
1	0
0,1	-20
0,01	-40
0,001	-60

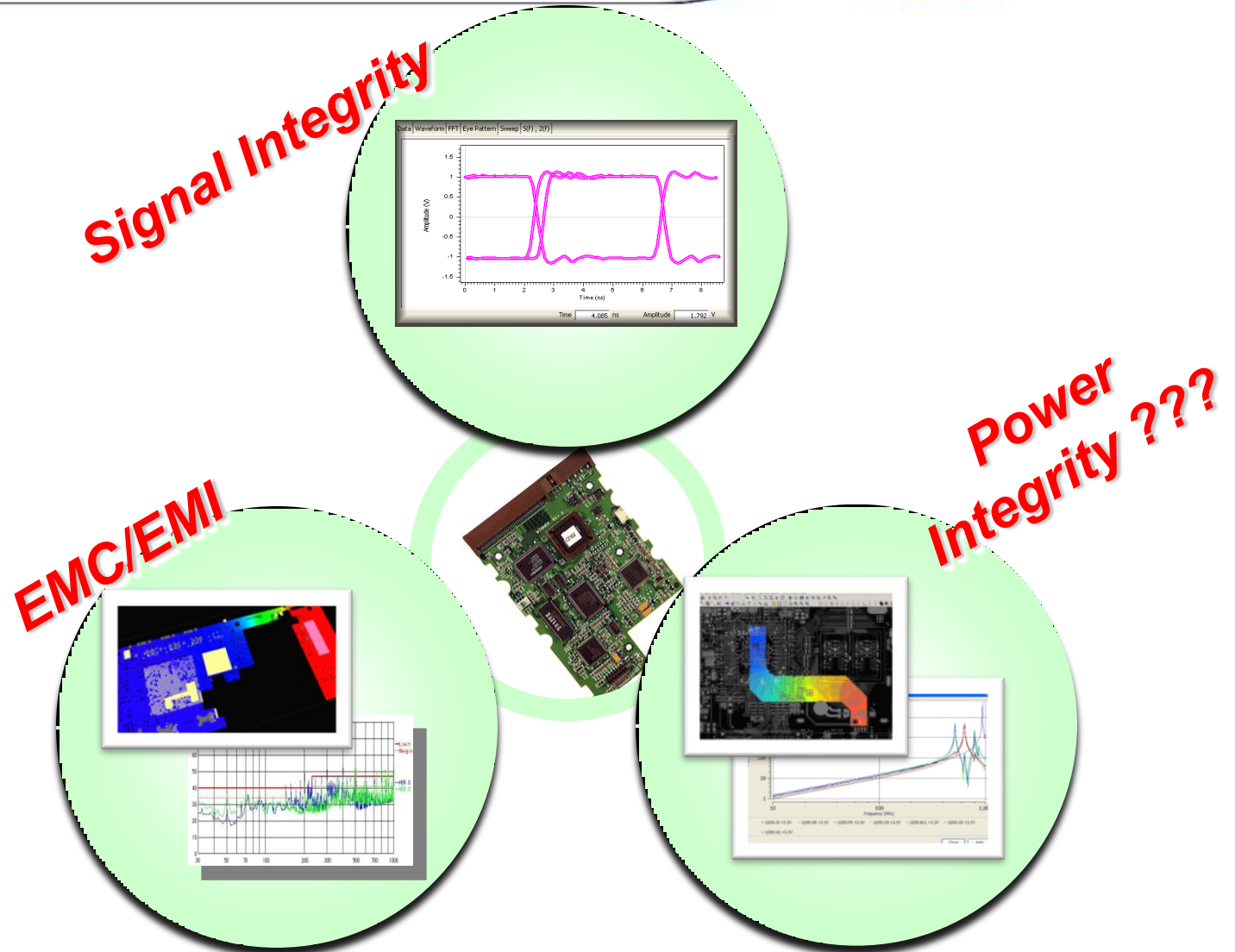


# Electronic Design Trends



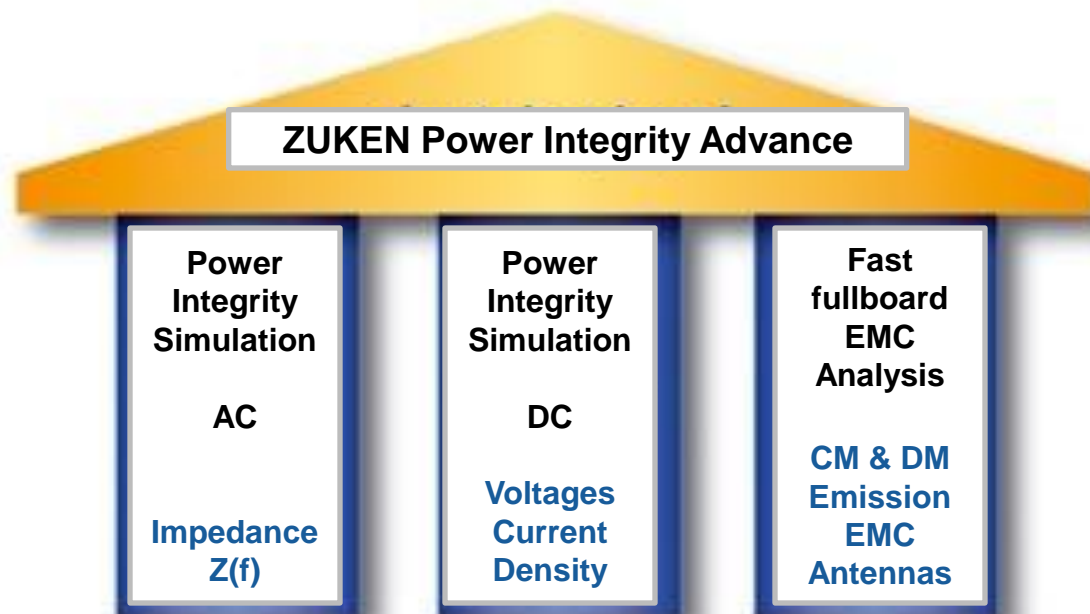


# The Good Old Days: Verification Disciplines separated (or not needed at all)



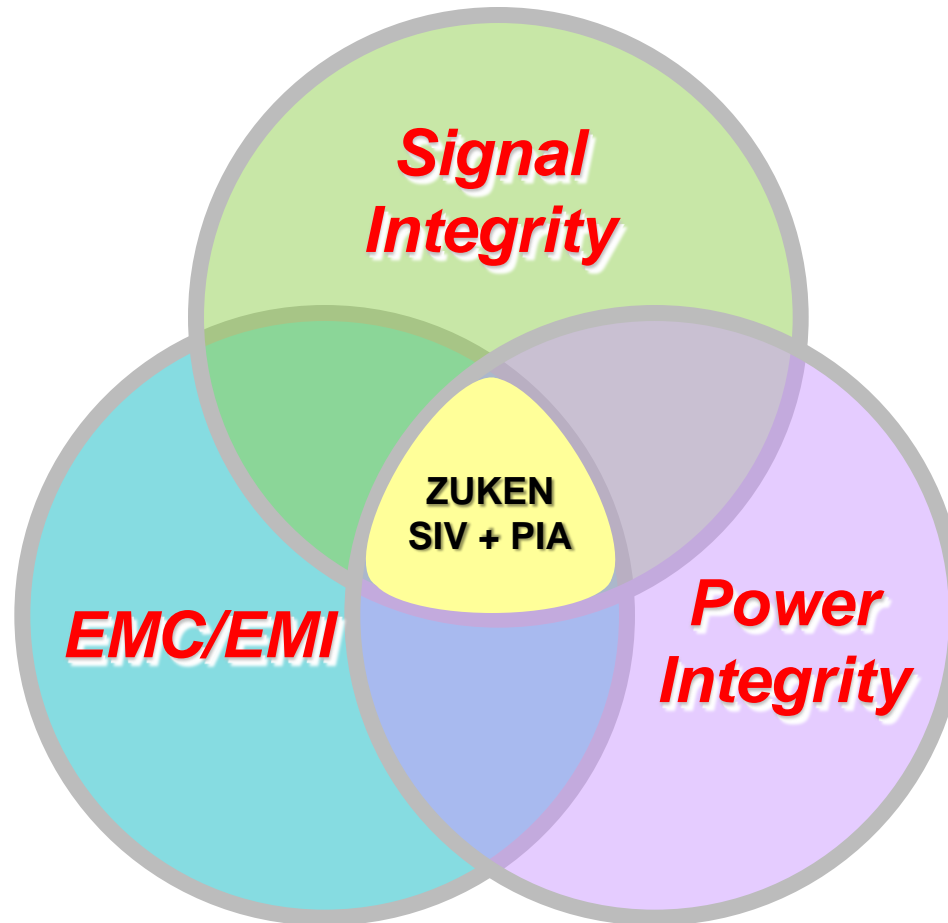


# The 3 Functional Columns of Power Integrity Advance



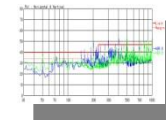
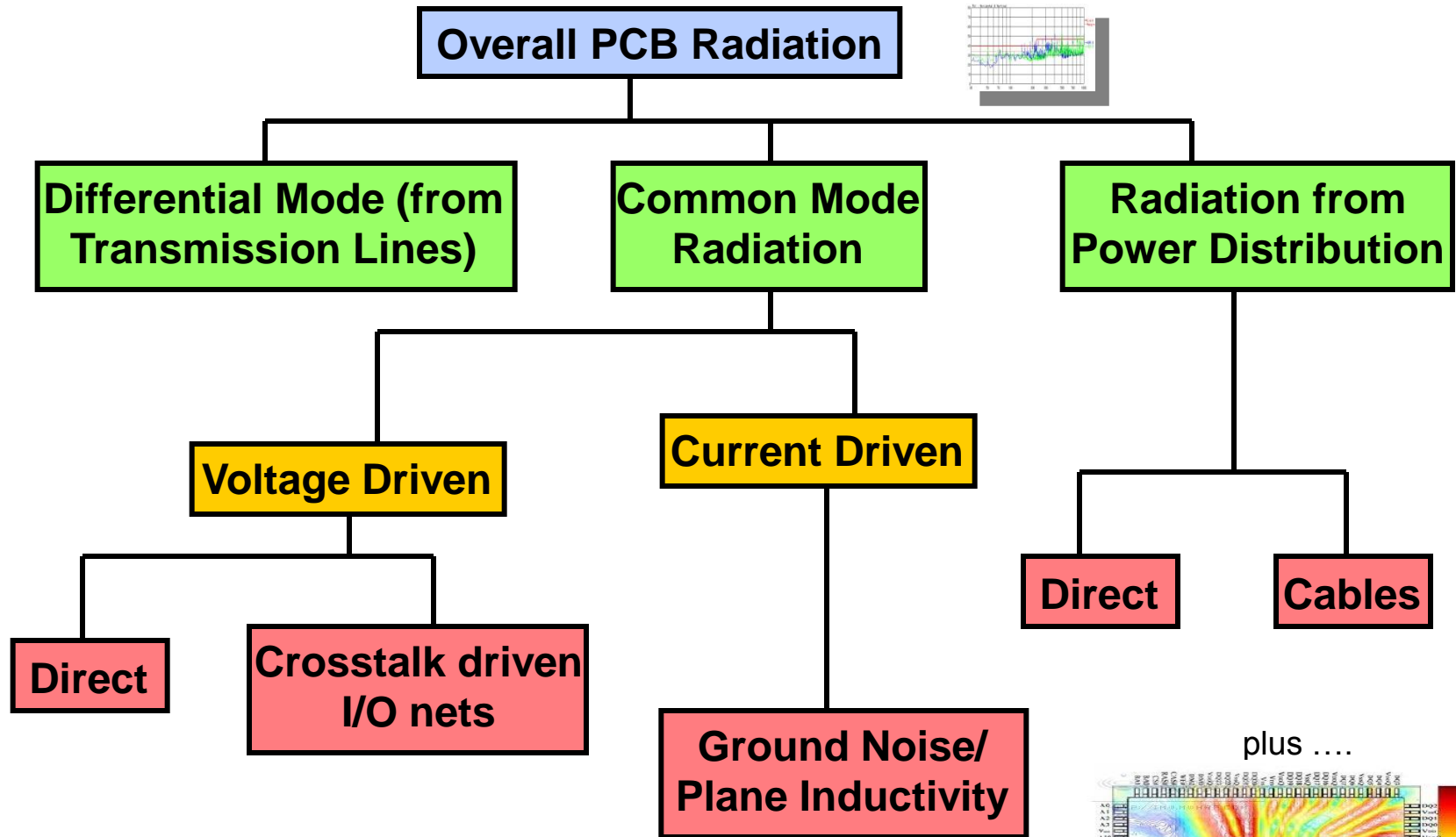


# Today: Concurrent Approach Needed





# → What causes PCBs to radiate ...

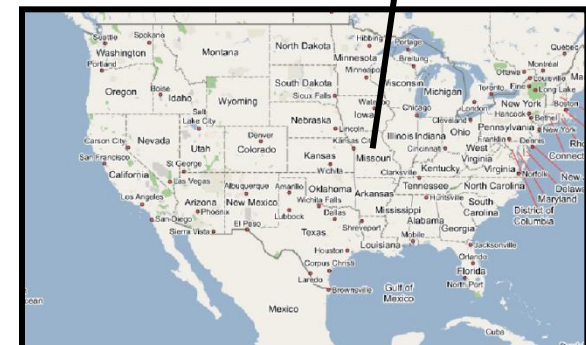




# The Idea behind: UMR EMC-Expert System Approach



- Modular *new* approach to EMC analysis: separated into single algorithms, covering a specific EMI effect, individually
- Based on available information about ICs, (i.e., circuit models, IBIS)
- Therefore shares/utitlizes information which might be already inhouse (SI simulation process)
- Treating:
  - ✓ **Differential- & common mode radiation**
  - ✓ **Power Bus analysis**
- Verified by measurements & numerical computations (at UMR and their partners)
- Goals:
  - Fast identification of critical areas & configurations
  - Estimation of potential radiation levels
  - Usable within the design-flow, by **non-experts**, too!





# The EMC-Expert System Approach

## The EMC Expert System Consortium



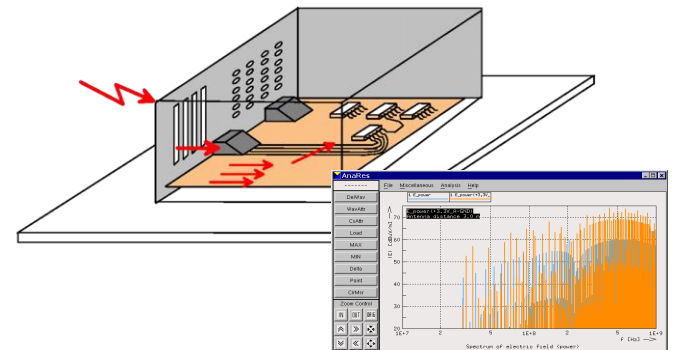
- Mission of the University of Missouri Rolla (UMR) Expert System Consortium (EMC Consortium):

*The software looks for EMI antennas on or off the board and evaluates how hard they are being driven. It identifies any problems found with the board layout and estimates the impact of these problems on the radiated EMI from the system*

Source: [www.emclab.umr.edu/consortium](http://www.emclab.umr.edu/consortium)



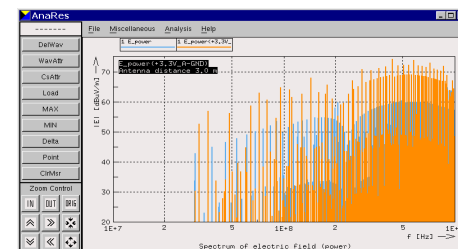
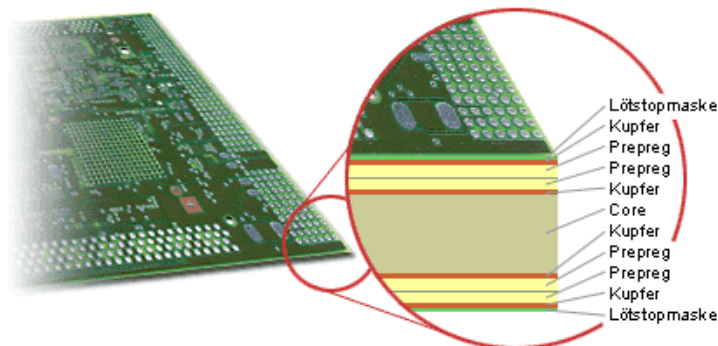
- Zuken is a member of this Consortium since 1996. Other members include:
  - Apple Computer Corporation, IBM Corporation, Intel, LG Corporation, Mentor Graphics, NEC Corporation, NCR, Siemens, Sony Corporation
- Current research of the EMC Consortium
  - System Level EMI predictions
  - DC Power Bus analysis
  - ESD related analysis
  - ...





# The EMC-Expert System Approach

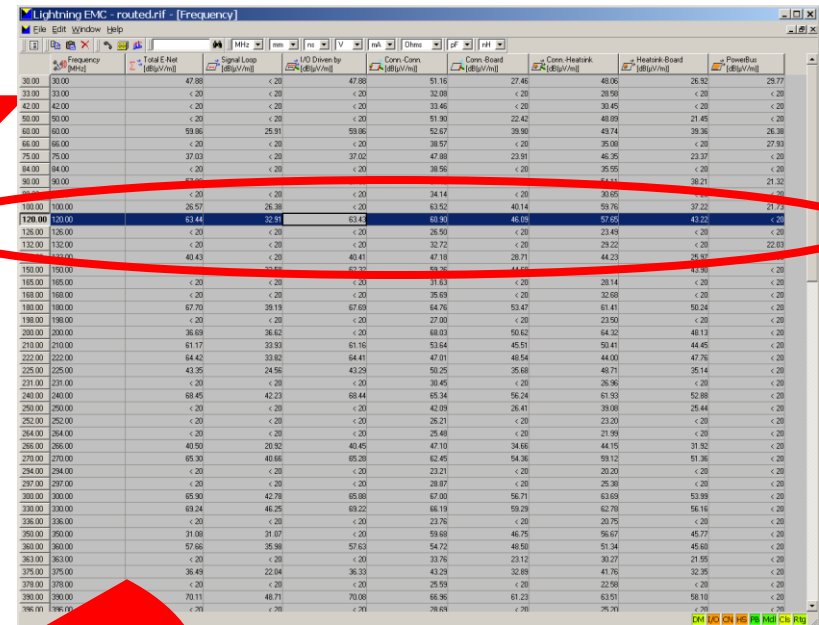
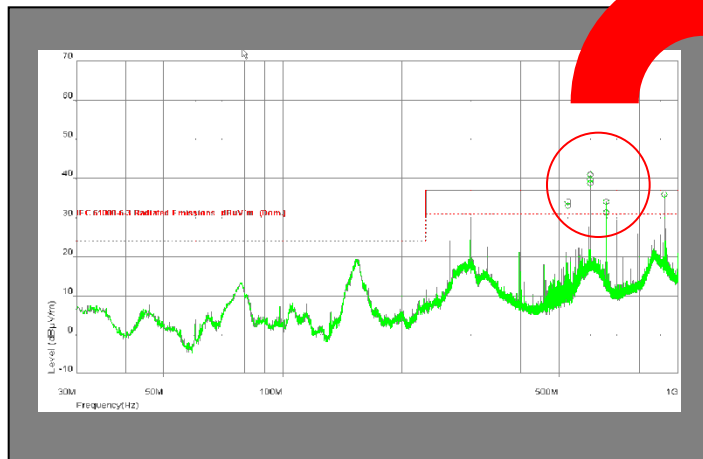
- The *EMC Expert System approach* intends to *simulate* the way how a human EMC expert will treat/solve EMC problems.
- Its not intended to compete against measurement and/or 3D solvers (as human experts won't do either)
- Its not solving Maxwell (as human experts don't do either – most of them).
- Its all about:
  - Looking the whole board at once
  - Identify and qualify potential antennas
  - Know/propose how to get rid of them
  - Predict the effectiveness of a measure with respect to EMC/far field





# PIA EMC&PI: Noise/Problem Source Identification

Goal: Identification of sources, contributing effects and configurations to a specific peak in the spectrum, feedback to CAD layout



The screenshot shows a table titled 'Lightning EMC - routed.rtf - [Frequency]'. The table has multiple columns for different EMC parameters, including Frequency, Total E-Field, Signal Loop, I/O Driven by, Conn. Board, Conn. Board, Conn. Board, Conn. Board, Conn. Board, and PowerBus. The table lists values for various frequency ranges, with a red circle highlighting the 100M to 150M Hz range.

Frequency (Hz)	Total E-Field (dBµV/m)	Signal Loop (dBµV/m)	I/O Driven by (dBµV/m)	Conn. Board (dBµV/m)	Conn. Board (dBµV/m)	Conn. Board (dBµV/m)	Conn. Board (dBµV/m)	Conn. Board (dBµV/m)	PowerBus (dBµV/m)
30.00	30.00	47.88	< 20	47.88	51.16	27.48	40.06	26.92	29.77
33.00	33.00	< 20	< 20	< 20	32.08	< 20	28.98	< 20	< 20
42.00	42.00	< 20	< 20	< 20	33.46	< 20	30.45	< 20	< 20
50.00	50.00	< 20	< 20	< 20	31.90	22.42	40.89	21.45	< 20
60.00	60.00	59.86	25.91	59.86	52.67	39.90	43.74	39.96	26.38
66.00	66.00	< 20	< 20	< 20	38.57	< 20	35.08	< 20	27.93
75.00	75.00	37.03	< 20	37.02	47.88	23.91	46.35	23.37	< 20
84.00	84.00	< 20	< 20	< 20	38.96	< 20	35.95	< 20	< 20
90.00	90.00	< 20	< 20	< 20	34.14	< 20	30.65	< 20	21.32
100.00	100.00	26.57	26.36	< 20	63.52	40.14	59.76	37.22	21.73
120.00	120.00	63.44	32.91	63.43	46.68	57.65	43.22	< 20	< 20
125.00	125.00	< 20	< 20	< 20	26.50	< 20	23.49	< 20	< 20
132.00	132.00	< 20	< 20	< 20	32.72	< 20	29.22	< 20	23.03
150.00	150.00	40.43	< 20	40.41	47.18	39.71	44.23	26.57	< 20
160.00	160.00	< 20	< 20	< 20	31.63	< 20	28.14	< 20	< 20
180.00	180.00	< 20	< 20	< 20	26.69	< 20	22.60	< 20	< 20
188.00	188.00	67.70	39.19	67.69	64.76	53.47	61.41	50.24	< 20
198.00	198.00	< 20	< 20	< 20	27.00	< 20	23.50	< 20	< 20
200.00	200.00	36.69	36.62	< 20	68.03	50.62	64.32	48.13	< 20
210.00	210.00	61.17	33.93	61.16	53.64	45.51	50.41	44.45	< 20
220.00	220.00	64.42	33.82	64.41	47.81	45.54	44.00	47.76	< 20
225.00	225.00	43.35	24.56	43.29	50.25	35.68	49.71	35.14	< 20
230.00	230.00	< 20	< 20	< 20	30.45	< 20	26.96	< 20	< 20
240.00	240.00	68.45	42.23	68.44	65.34	56.24	61.93	52.88	< 20
250.00	250.00	< 20	< 20	< 20	42.09	26.41	39.08	25.44	< 20
252.00	252.00	< 20	< 20	< 20	26.21	< 20	23.30	< 20	< 20
264.00	264.00	< 20	< 20	< 20	25.48	< 20	21.99	< 20	< 20
266.00	266.00	40.50	20.92	40.45	47.10	34.66	44.15	31.92	< 20
270.00	270.00	65.30	40.66	65.28	62.49	54.36	59.12	51.36	< 20
284.00	284.00	< 20	< 20	< 20	22.21	< 20	20.20	< 20	< 20
297.00	297.00	< 20	< 20	< 20	28.87	< 20	25.38	< 20	< 20
300.00	300.00	65.90	42.78	65.88	67.00	56.71	63.69	53.99	< 20
330.00	330.00	69.24	46.25	69.22	66.19	59.29	62.70	56.16	< 20
336.00	336.00	< 20	< 20	< 20	23.76	< 20	20.75	< 20	< 20
360.00	360.00	71.88	31.07	71.86	66.76	59.68	66.47	45.77	< 20
360.00	360.00	57.66	35.98	57.63	54.72	48.50	51.34	45.60	< 20
363.00	363.00	< 20	< 20	< 20	33.76	23.12	30.27	21.95	< 20
375.00	375.00	36.49	22.04	36.33	43.29	32.89	41.76	32.35	< 20
378.00	378.00	< 20	< 20	< 20	25.93	< 20	22.98	< 20	< 20
380.00	380.00	70.11	40.71	70.09	66.96	61.23	63.51	56.10	< 20
390.00	390.00	< 20	< 20	< 20	29.69	< 20	26.90	< 20	< 20

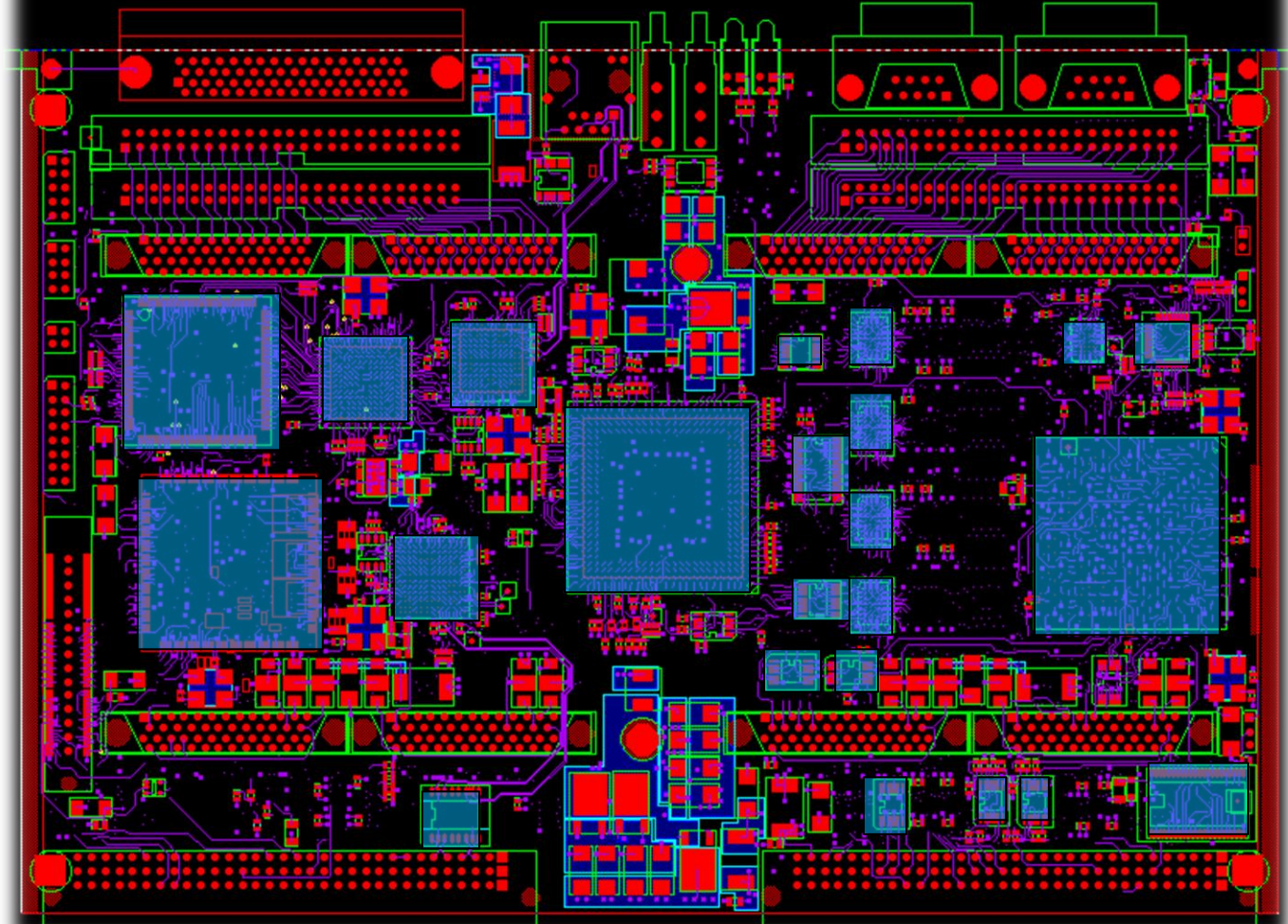




# A typical PCB ....

(from 2009, industry automation, Power-PC & DDR Memory)

- The active devices (ICs) will consume the majority of the energy
- They need the various voltage levels to work (on this board 17 different supply and ground nets)
- Several BGAs are used on this design



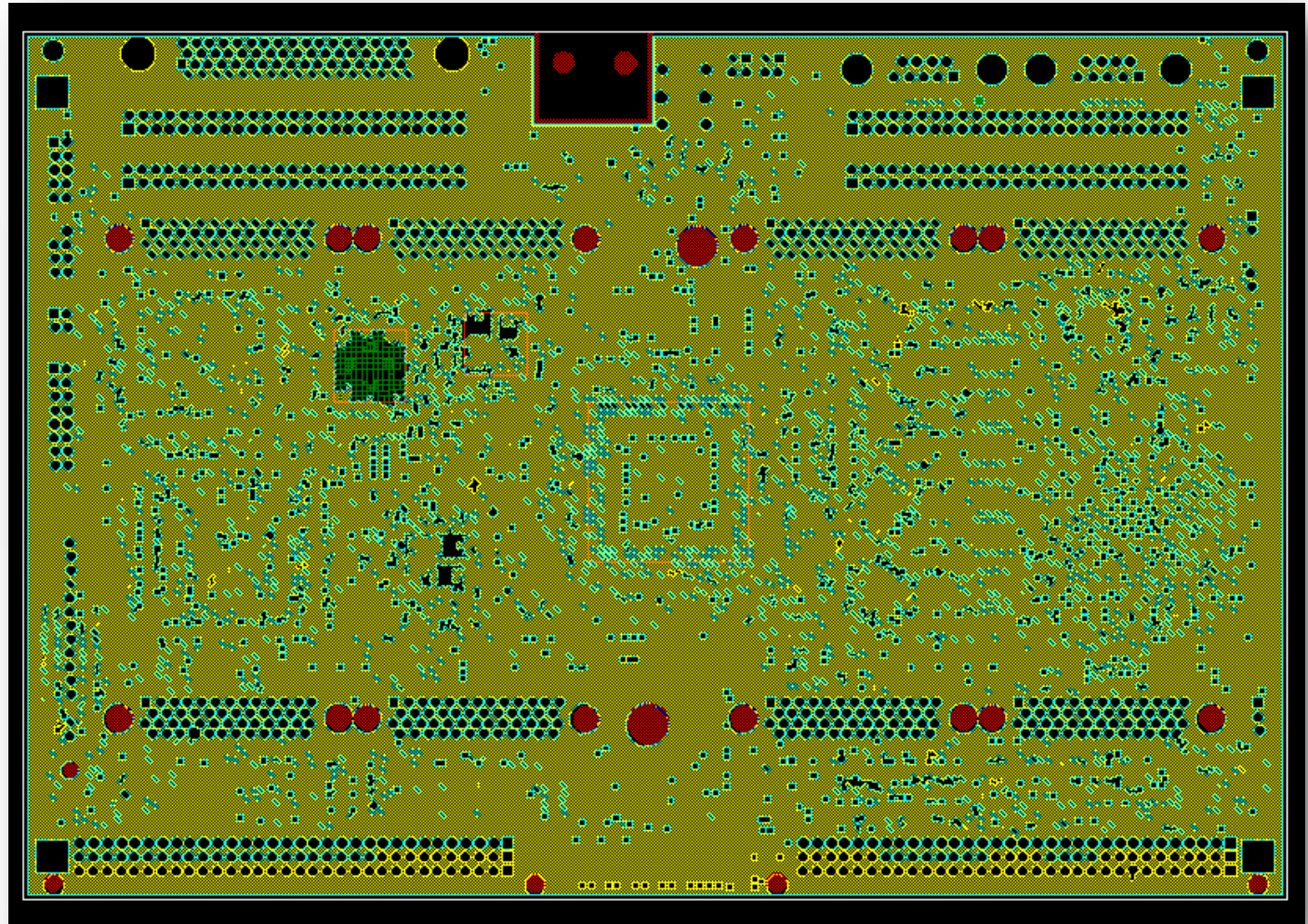


So most of our digital PCBs have things like this .... (hopefully)

What is this ???

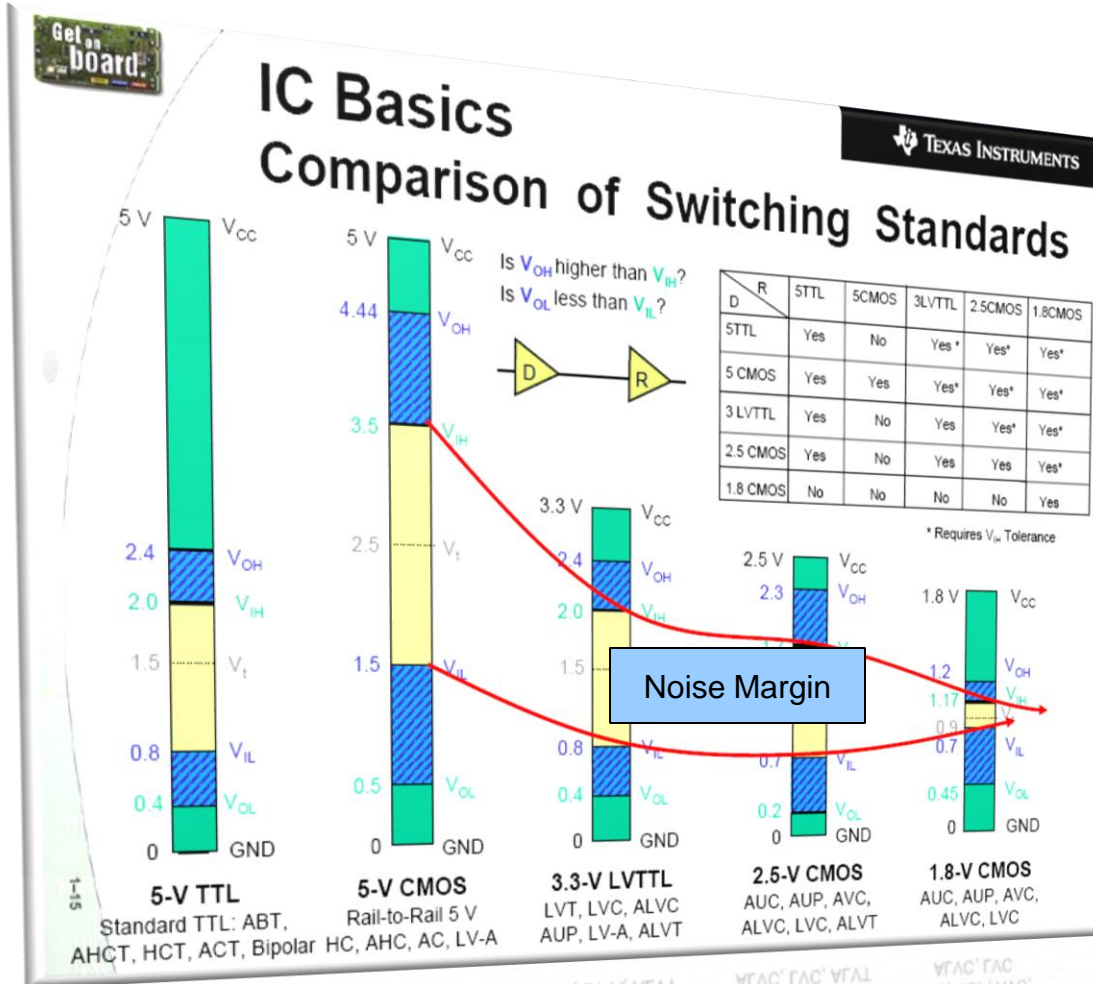


A power  
distribution  
system  
(PDS)



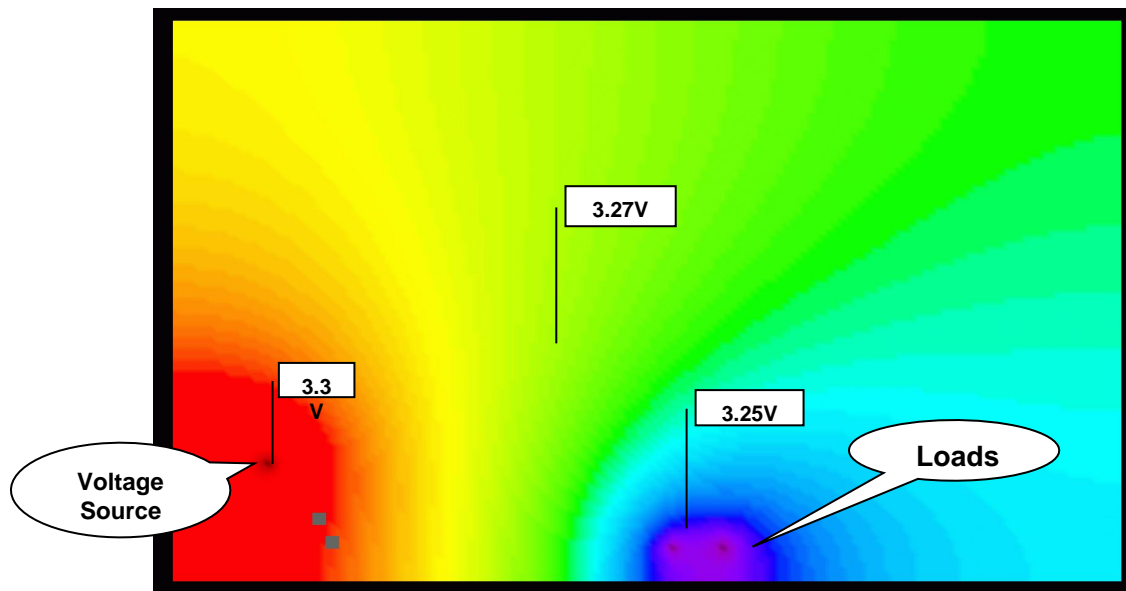


# Lowered Noise Margins of today's ICs





Voltages are not equally distributed and not considered ideal over copper planes

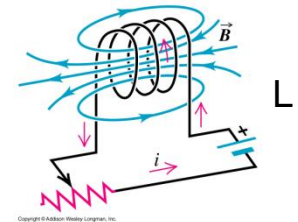
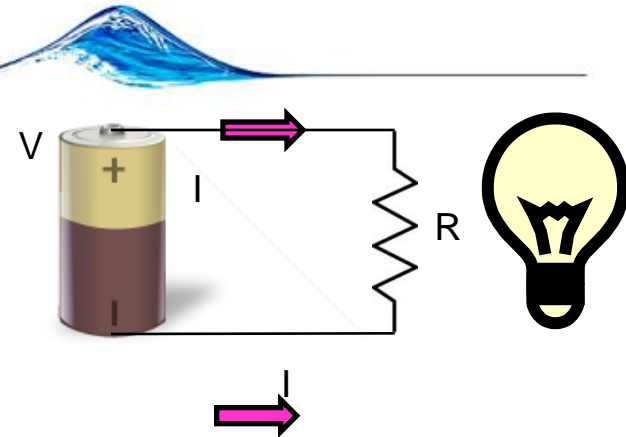


*Example: 3.3V Power Distribution System*

“Voltage drops” occur on the copper area and within the vias – but why ?



# Basic Electrical Concepts #1

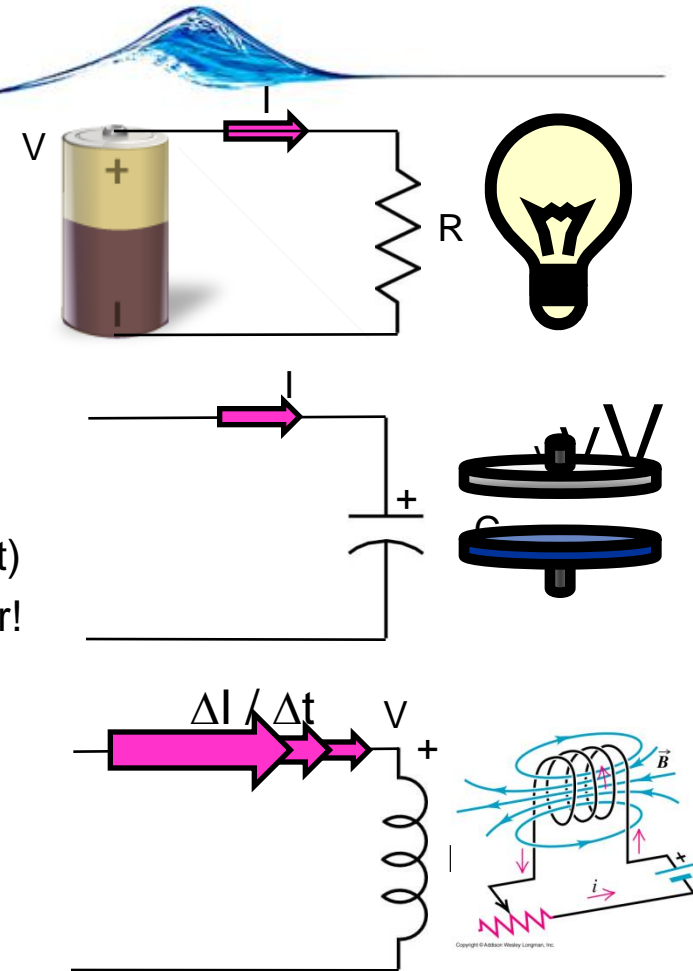


- Voltage: **Electrical potential difference** (denoted  $\Delta V$  and measured in volts) between two points. A voltage may represent either a source of energy (electromotive force) or it may represent lost or stored energy (potential drop). Voltage can be caused by static electric fields, by electric current through a magnetic field, by time-varying magnetic fields, or a combination of all three.
- Current: **Electric current** is a flow of electric charge through a medium. This charge is typically carried by moving electrons in a conductor such as wire. An electric current (Amperes law) produces a magnetic field.
- No voltage without current, no current without voltage
- **Ground:** Not an acceptable technical term at all (current return path is what should be used, Dr. Archembault from IBM invented the phrase that ground is a **place to plant potatoes or carrots**), so there even as well does not exist a “Ground-Bouncing” like people assume it to happen, it’s a narrowing of the potential difference



# Basic Electrical Concepts #2

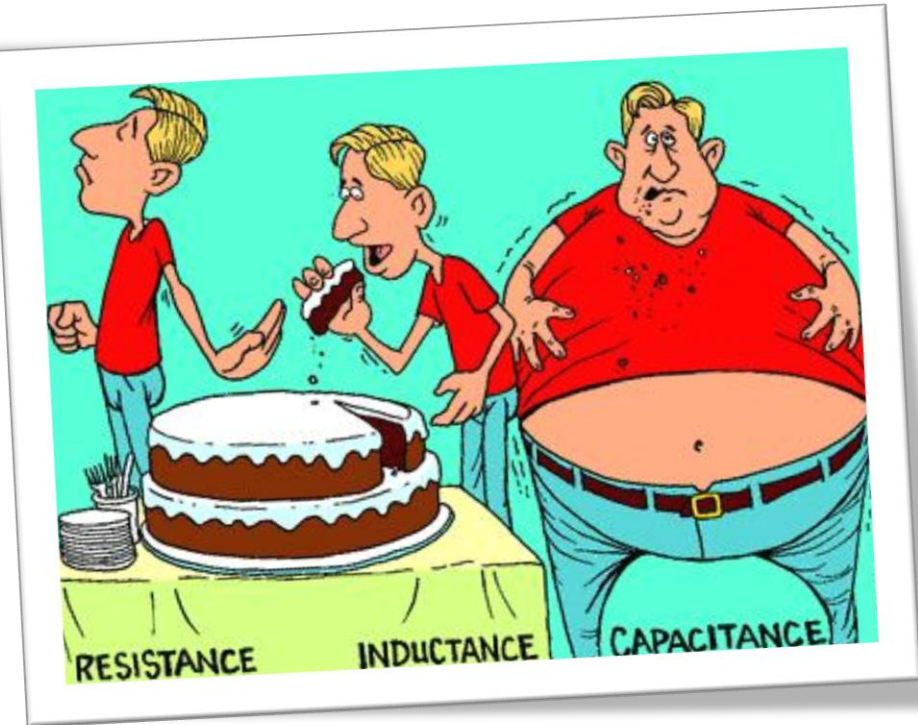
- Resistors dissipate **energy**
  - Resistance = Voltage / Current ( $R = V / I$ )
  - Voltage = Current \* Resistance ( $V = I * R$ )
- Capacitors store **energy** in an electric field
  - Charge = Capacitance \* Voltage ( $q = CV$ )
  - Current ( $\Delta q / \Delta \text{time}$ ) =  $C * (\Delta V / \Delta t)$  ( $I = C * \Delta V / \Delta t$ )
  - Power plane over ground plane is a great capacitor!
- Inductors store **energy** in a magnetic field
  - Voltage = Inductance \*  $(\Delta I / \Delta t)$  ( $V = L * \Delta I / \Delta t$ )
  - Oppose current changes with a voltage
  - Inductive kick: pull the plug on a vacuum cleaner when it's running!





# Basic Electrical Concepts #3

- For Signal Integrity you should care for resistances and capacitances
- For Power Integrity, **Mr. Inductance** is the guy to care for
- Requirements do increase (i.e. JEDEC DDRx)



Picture © Agilent

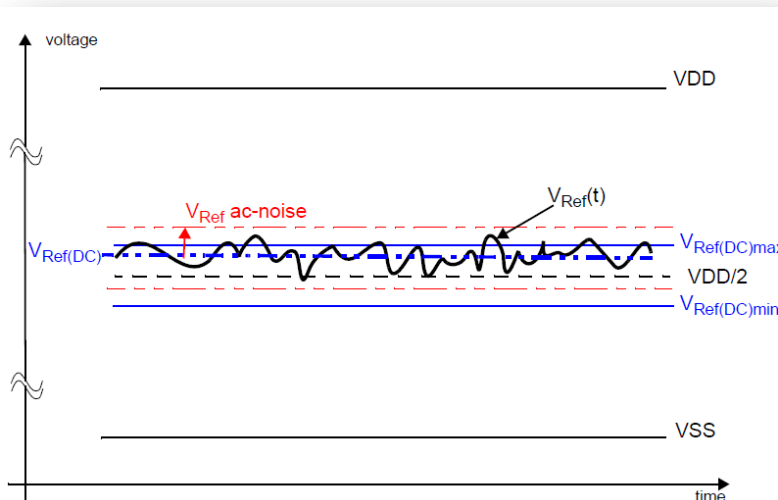
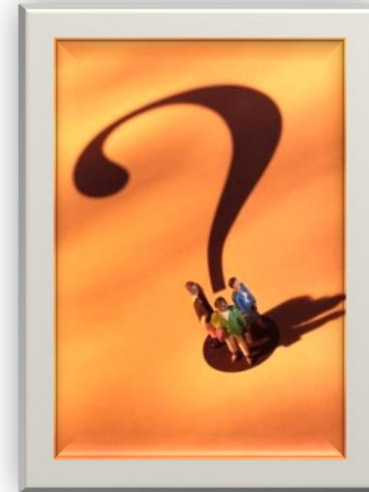
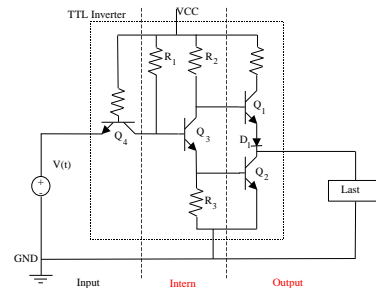
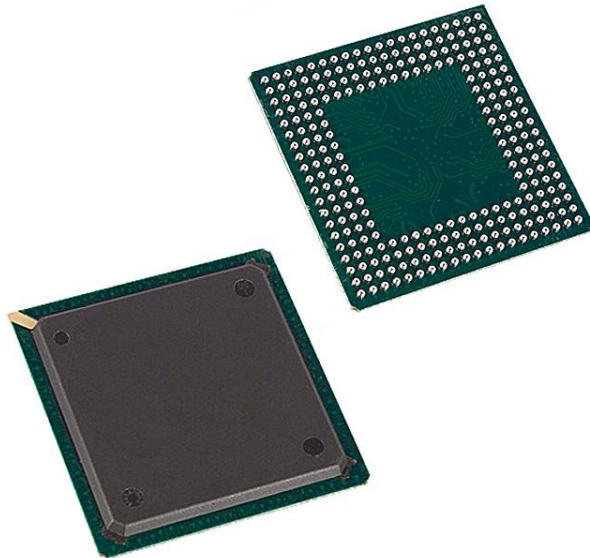


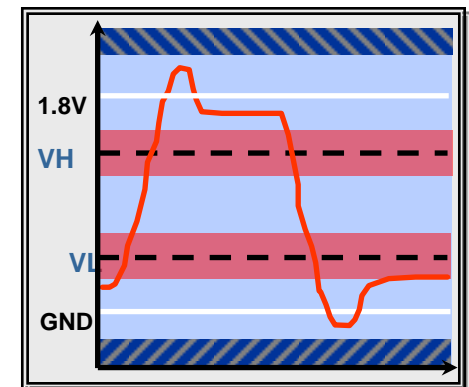
Figure 90 — Illustration of  $V_{Ref(DC)}$  tolerance and  $V_{Ref}$  ac-noise limits



# When Integrated Circuits Switch ....



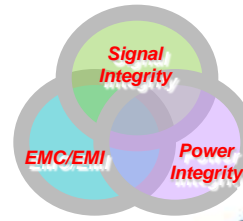
- They (should) change logic state.
- They need **charge**.
- **Voltage** has to be delivered (for reaching logic levels).
- A switching **current** will occur !



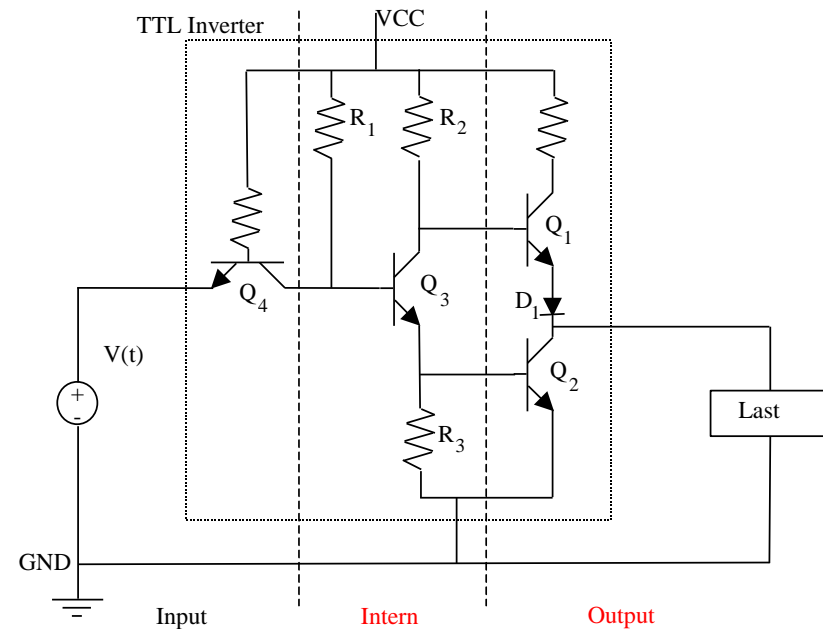
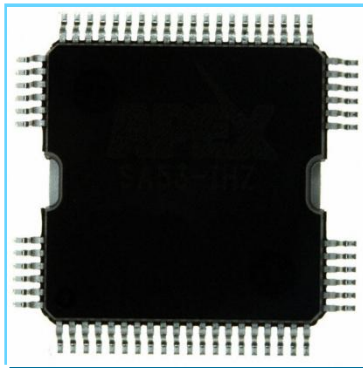
Relation between voltage & current ? → **Ohm's law**



# Power Integrity: Switching Current



- IC Switching *current* depends on:
  - Number of active outputs
  - Activity state
  - Driver rise and fall times
  - Clock frequencies
  - Load conditions





# Do you have to worry ?

It depends ... but I think YES !

Design *Challenges* increase dramatically !

(Example: Xilinx design guides for Xilinx Spartan FPGAs)

## PDS Design for FPGAs

- One capacitor per Vcc pin
- Yes, EVERY Vcc pin – Vccint, Vcco, Vccaux, Vref
- Within the total count for each supply:
  - Allocate some in each frequency range
    - 3% 680 uF
    - 7% 2.2 uF
    - 15% 0.22 uF
    - 25% 0.047 uF
    - 50% 0.001 uF
- Power planes and/or sandwiches are a must



Power Planes

Power Planes

The Spartan-3E high-speed design successfully uses a one-layer, triple split plane. One quadrant of the design is shown in Figure 7. The design has 200-300 ps edge rates and a switching noise of 80 simultaneously switching LVCMOS 3.3V I/Os.




Figure 7: One Quadrant of the One-Layer, Triple Split Plane

The final plane requirements are determined by the required I/O and V<sub>DDQ</sub> voltages. If the V<sub>DDQ</sub> voltage is 2.5V, the layout is simple because only two planes are required. An example split plane is shown in Figure 8. Plane requirements may also be driven by other SI concerns, such as the need to avoid shapes that resonate at selected frequencies or the need to avoid splits when routing traces on adjacent layers.

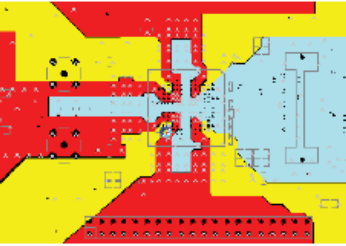


Figure 8: Example Split Plane

XAPP489 (v1.0) October 31, 2006
[www.xilinx.com](http://www.xilinx.com)
6

Pictures © Xilinx



# Evolution of Power Distribution Systems

- The requirements on power distribution systems have changed in the last 20 years.
- CMOS voltages are decreasing while more pins can switch simultaneously, inducing serious switching current (and more power consumption), at higher frequencies.
- Matching the *target impedance* (ratio of voltage/current while switching) the power distribution system is a key problem in modern high speed designs.

Year	Voltage (V)	Current (A)	Max-Pins (IC)	$Z_{\text{target}}$ (m $\Omega$ )	f [MHz]
1990	5	1	68	250	16
1994	3.3	3	244	50	66
1998	2.5	12	>500	10	233
2002	1.8	50	>1200	2	800
2006	1.5	> 100	> 2000	0.5 - 1	> 2GHz
2010	1.0	Several hundred	> 4000	<< 1	> 3 GHz



# Basic Electrical Concepts #4

- We do have the relation between voltages (to be supplied) and currents (occurring) → Ohms law describes that can be applied for the relation between voltage, current and impedance
- Resistance in the PCB design world goes to become impedance (ratio between voltage and current in the switching process)
- Please Note: This is a different impedance the characteristic impedance of signal traces (means, computed differently)
- Silicon vendors nowadays define  $Z_{\text{target}}$  as requirement/constraint

Table 1. PowerPC Processor Parameters

Processor	Parameter							No. of $V_{DD}$ pins	Notes
	$V_{\text{SUPPLY}}$	$P_{\text{MAX}}$	$I_{\text{MAX}}$	$V_{\text{RIPPLE}}$	$V_{\text{RIPPLEPCT}}$	$di/dt$	$Z_{\text{TARGET}}$		
MPC8245 @ 300 MHz	1.8 V	2.2 W	1.22 A	± 100 mV	5.6%	0.1 A/ns	83 mΩ	20	1,2
MPC8245 @ 466 MHz	2.1 V	3.1 W	1.47 A	± 100 mV	4.8%	0.1 A/ns	69 mΩ	20	1
MPC7410 @ 500 MHz	1.8 V	11.9 W	6.61 A	± 100 mV	5.6%	0.2 A/ns	15 mΩ	18	1
MPC7445 @ 867 MHz	1.3 V	21.0 W	16.15 A	± 50 mV	3.9%	0.2 A/ns	3.1 mΩ	21	1
MPC7457 @ 1267 MHz	1.3 V	25.6 W	19.69 A	± 50 mV	3.9%	0.2 A/ns	2.6 mΩ	21	1,3
MPC7447A @ 1420 MHz	1.3 V	30.0 W	23.08 A	± 50 mV	3.9%	0.2 A/ns	2.2 mΩ	21	1

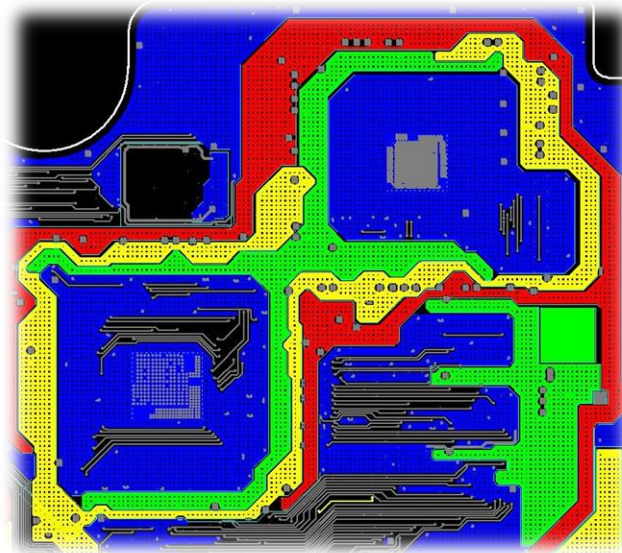
- The allowed voltage tolerance (voltage ripple) must be known/defined (usually around 5 %) to derive  $Z_{\text{target}}$

$$Z_{\text{Target}} = \frac{(\text{Power\_Supply\_Voltage}) \times (\text{Ripple\_Tolerance})}{\text{Dynamic\_Current}}$$



# Voltage Supply for ICs: Power Distribution System (PDS)

- The power distribution system (PDS) will provide voltages and deliver **charge** to the ICs on a PCB
- Charge on the board must be supplied over a broad frequency range:
  - Low frequency activities (we still have them)
  - In MHz range for CPU-peripheral interfaces
  - At the clock frequency (several hundreds of MHz)
  - **Provide a low impedance path for parasitic voltages at various harmonics of the clock**





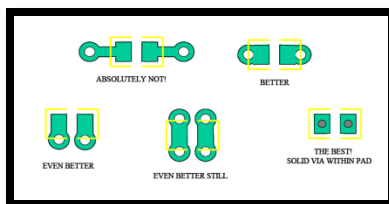
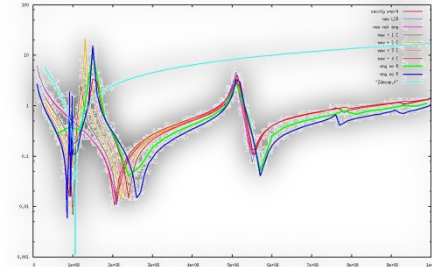
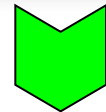
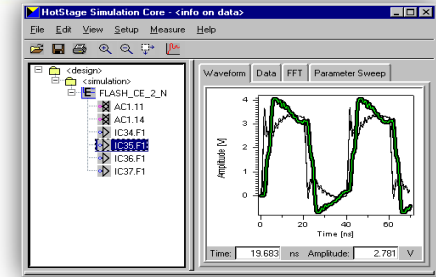
# Power Integrity Objective

Power Integrity ?

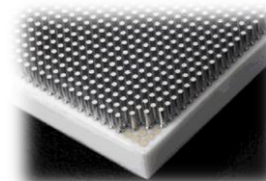
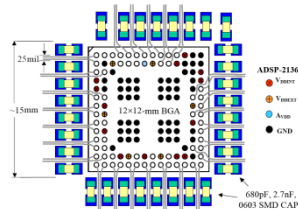
Power Integrity ⇔ Ensure proper behaviour of power distribution systems (PDS) (ako *Integrity* behaviour of power supply system)

PCB Design today → Increasing challenges, complexity is growing continuously:

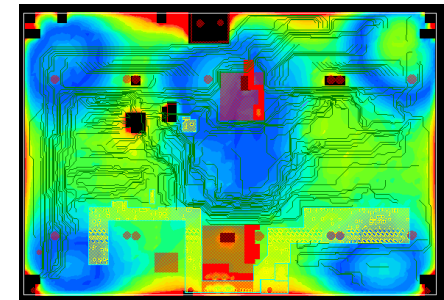
- Faster data rates (i.e. serial interconnects)
- Super-complex devices (several 1000 pins)
- Very fast memory interfaces (DDR2 interfaces common, i.e. on ASIC cells and/or FPGAs)
- Increased number of power supplies (dozens)
- Increased power consumption, problems with large currents and thermal management
- Requirements beyond *classical* SI constraints (i.e. target impedances and decoupling requirements for CPUs or FPGAs)



Pictures © AMD and IBM

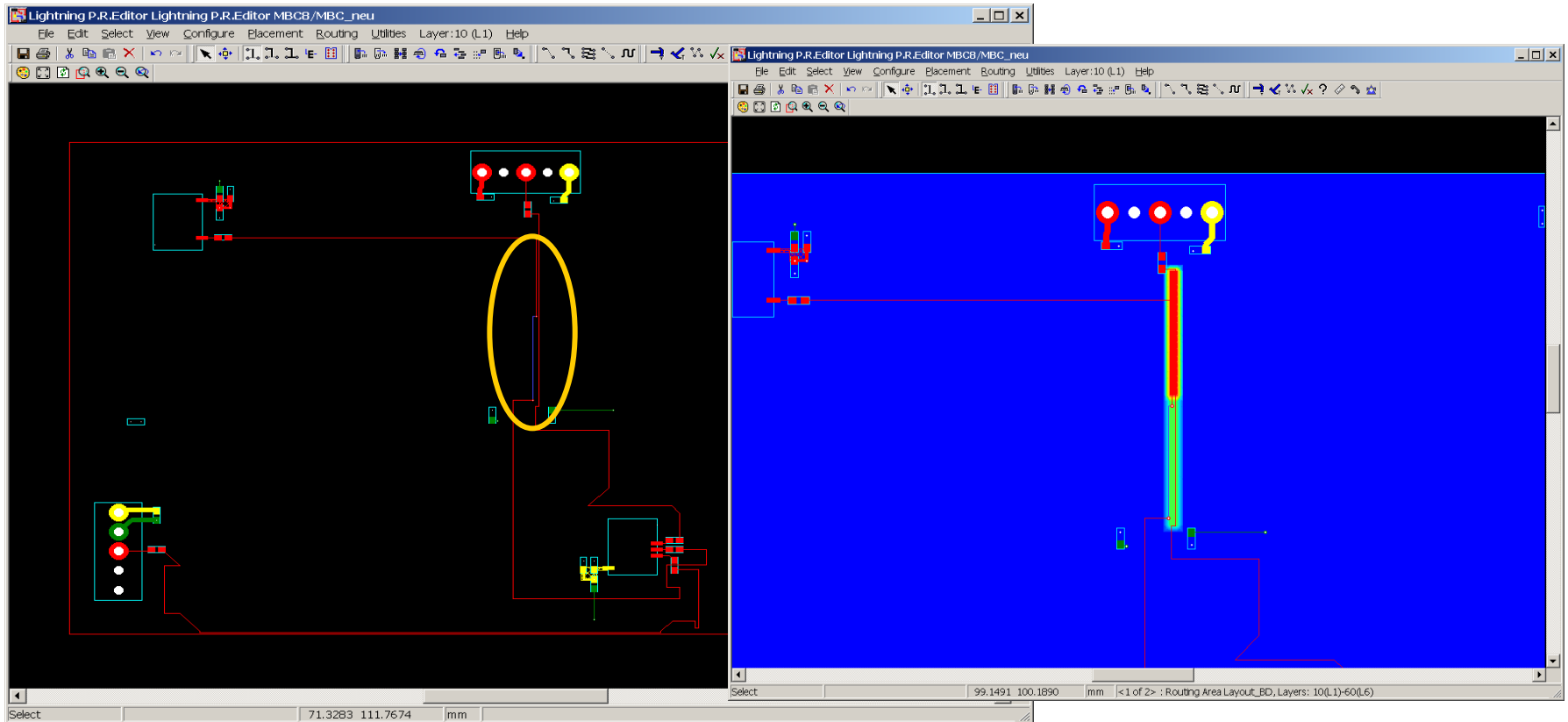


2577 pin CCGA





# EMC-What-Ifs: Show Field Hot-Spots & Coupling Voltages, fix problems on the fly



Lightning EMC - MBC\_neu.rif - [Radiation]

File Edit Simulation Window Help

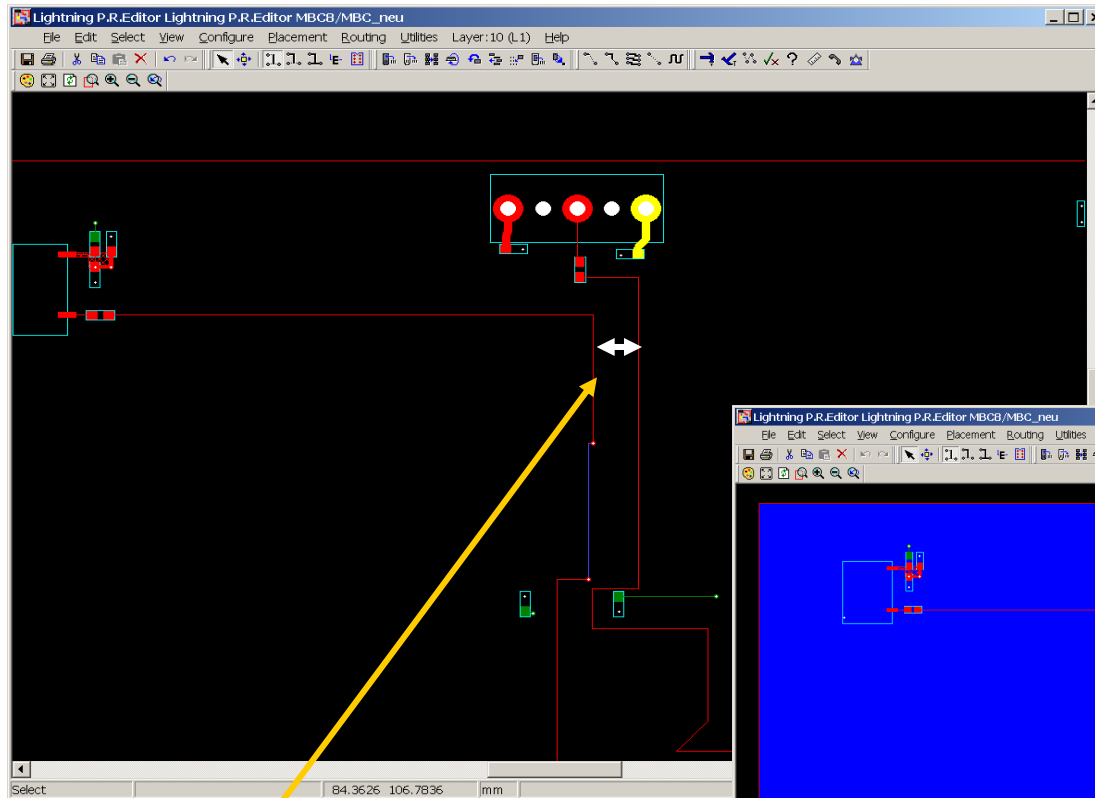
EMI Net EMI Connector EMI Heatsink

	E-Net	Total [dB(μV/m)]/[MHz]	Signal Loop [dB(μV/m)]/[MHz]	I/O Driven by [dB(μV/m)]/[MHz]	I/O Coupled to [dB(μV/m)]/[MHz]	V_CM [dB]/[MHz]
SIGN10_SIGN11_SIGN13	SIGN10_SIGN11_SIGN13	35.35 / 990.00	35.35 / 990.00		54.39 / 390.00 / SIGN7_SIGN8_SIGN9	0.00 / 390.00
SIGN14_SIGN4_SIGN5	SIGN14_SIGN4_SIGN5	50.05 / 390.00	< 20	50.05 / 390.00 / CN1	< 20	< -60 dB
SIGN7_SIGN8_SIGN9	SIGN7_SIGN8_SIGN9	54.39 / 390.00		54.39 / 390.00 / CN2		< -60 dB

DM I/O CN HS PB Md Cls Rtq

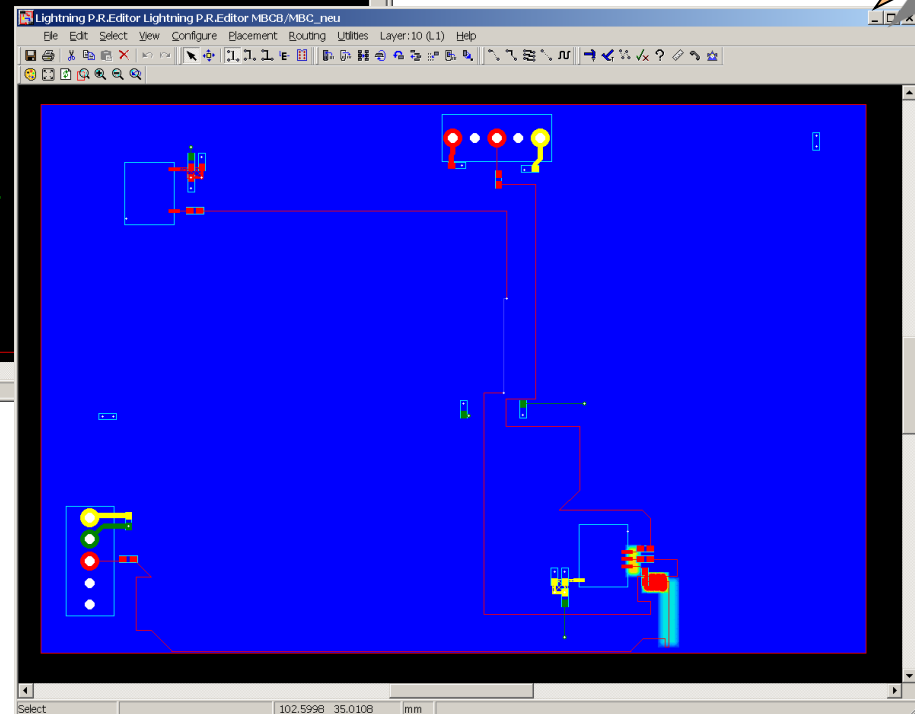


# EMC-What-Ifs: Show Field Hot-Spots & Coupling Voltages, fix problems on the fly



Increase spacing

Benefit  
Allow quick EMC-What-Ifs with respect to EMC noise caused by coupling structures.





What are the 4 key features of PIA EMC Analysis ?

1. It screens complete boards !
2. Its FAST (to be used in design process)
3. It identifies EMI sources (root causes) in form of structures on PCB (nets, ICs, connectors etc.)
4. It allows EMC and PI what-ifs





# Typical Ways of Treating EMC: Design Guidelines, Measurement (& Consultancy)

Typically during PCB design EMC issues are covered upfront by design guidelines and then in prototype stage by doing measurements.

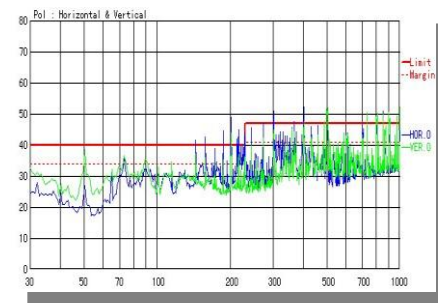
If this won't succeed, often external or internal EMC experts are asked for help.

But EMC Design rules will not make a good circuit board designer and measurement will not detect concrete error sources.

And, experts are limited/rare (and not cheap).

So designers should:

1. Use common sense !
2. Visualize and analyze signal current paths
3. Locate parasitic antennas and crosstalk paths
4. Be aware of potential EMI sources and antennas
5. Use software tools which will help/automate steps 1.-4.  
→ Lightning PIA EMC approach



$$\nabla \times H = J + \frac{\partial D}{\partial t}$$
$$\nabla \times E = -\frac{\partial B}{\partial t}$$

Maxwell Equations ?





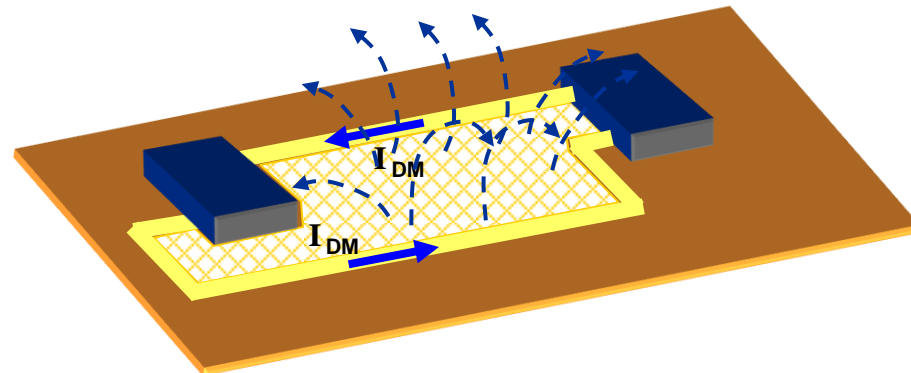
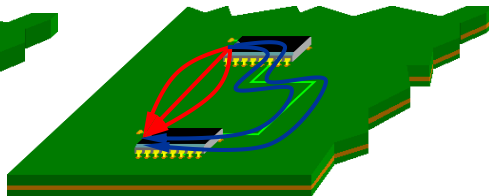
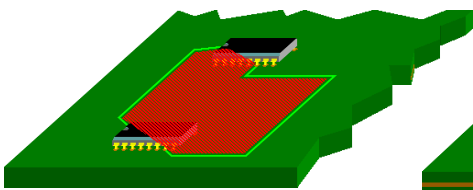
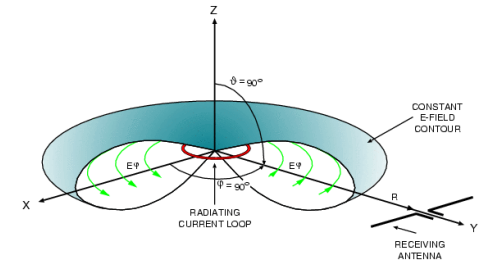
# EMC Mechanism: Differential Mode Radiation

Radiated emissions due to current loops created by signal traces and return paths

- Large current loops created by signal and GND traces
- GND planes decrease loop areas drastically

Main parameters are:

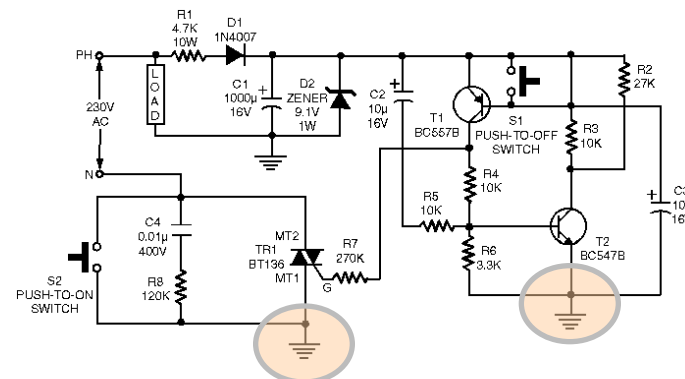
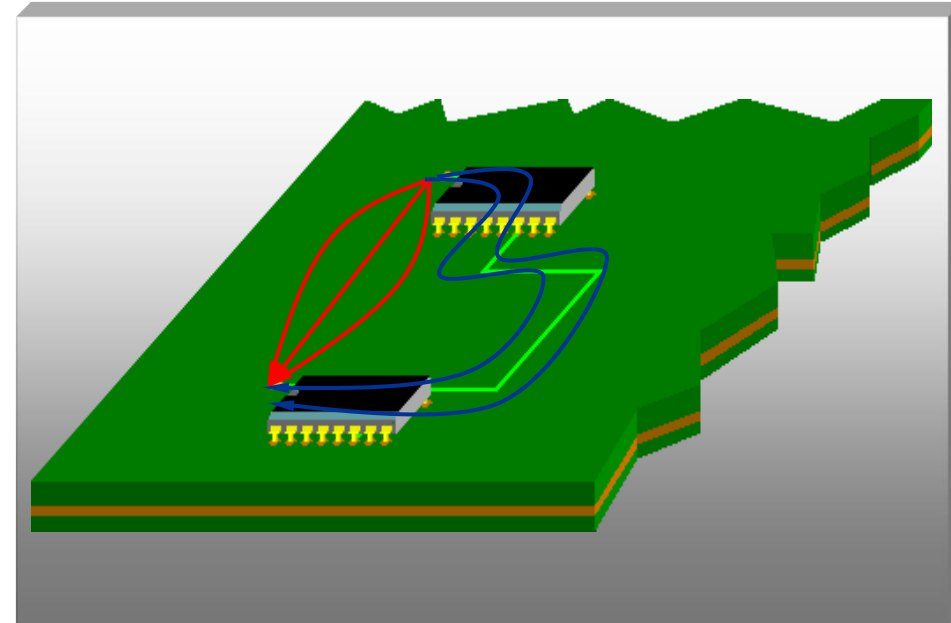
- Spectrum of the signal current  $I(f)$  (Driver, Receivers, Terminations, etc.)
- Frequency  $f$
- Loop Area  $A$  (distance to next reference plane of each net-segment)
- Distance to closest trace (trace length on top or bottom layer)





# Return Currents

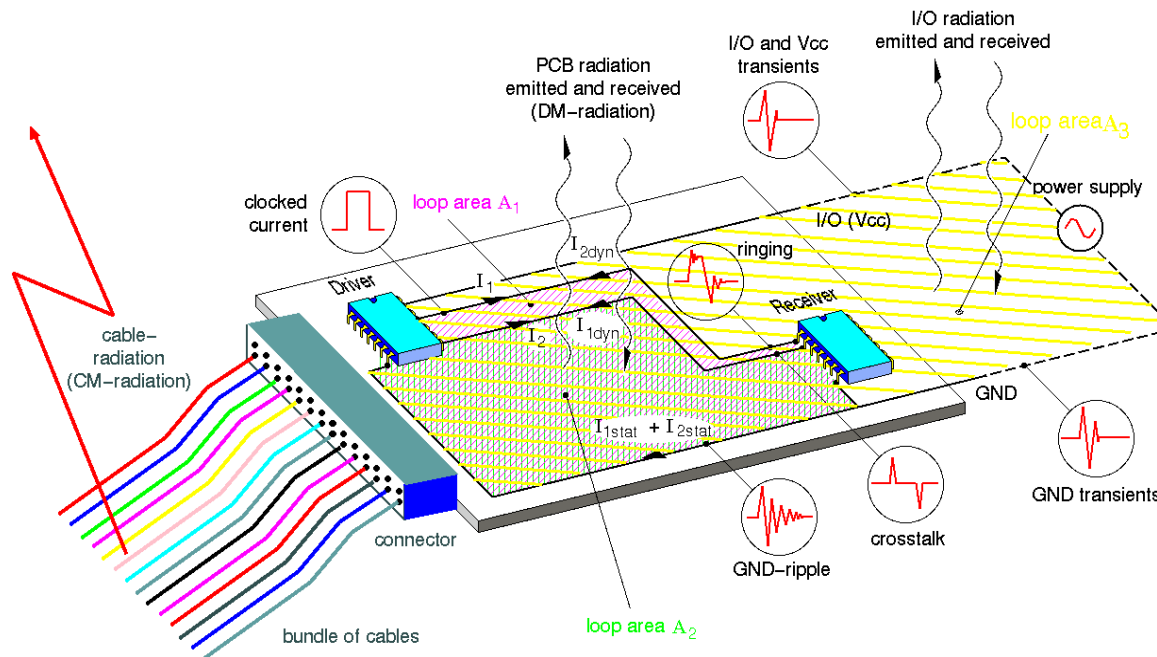
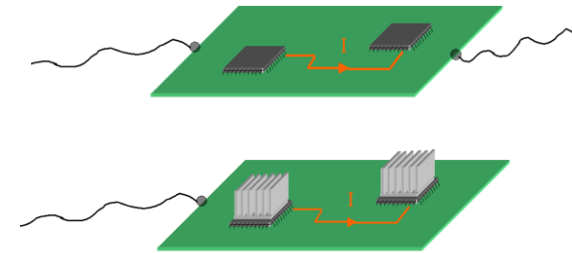
- Currents always returns to their source!
- They usually take the path:
  - of least impedance (for frequencies  $> 1\text{MHz}$ )
  - Not the path of the least resistance, only at very low frequencies, around  $10\text{ kHz}$ )
  - of course not the path of shortest distance or most convenient/nicest routing path
- Current loops create inductance !
- “Ground” is not an acceptable technical term.





# EMC Mechanism: Common Mode Radiation

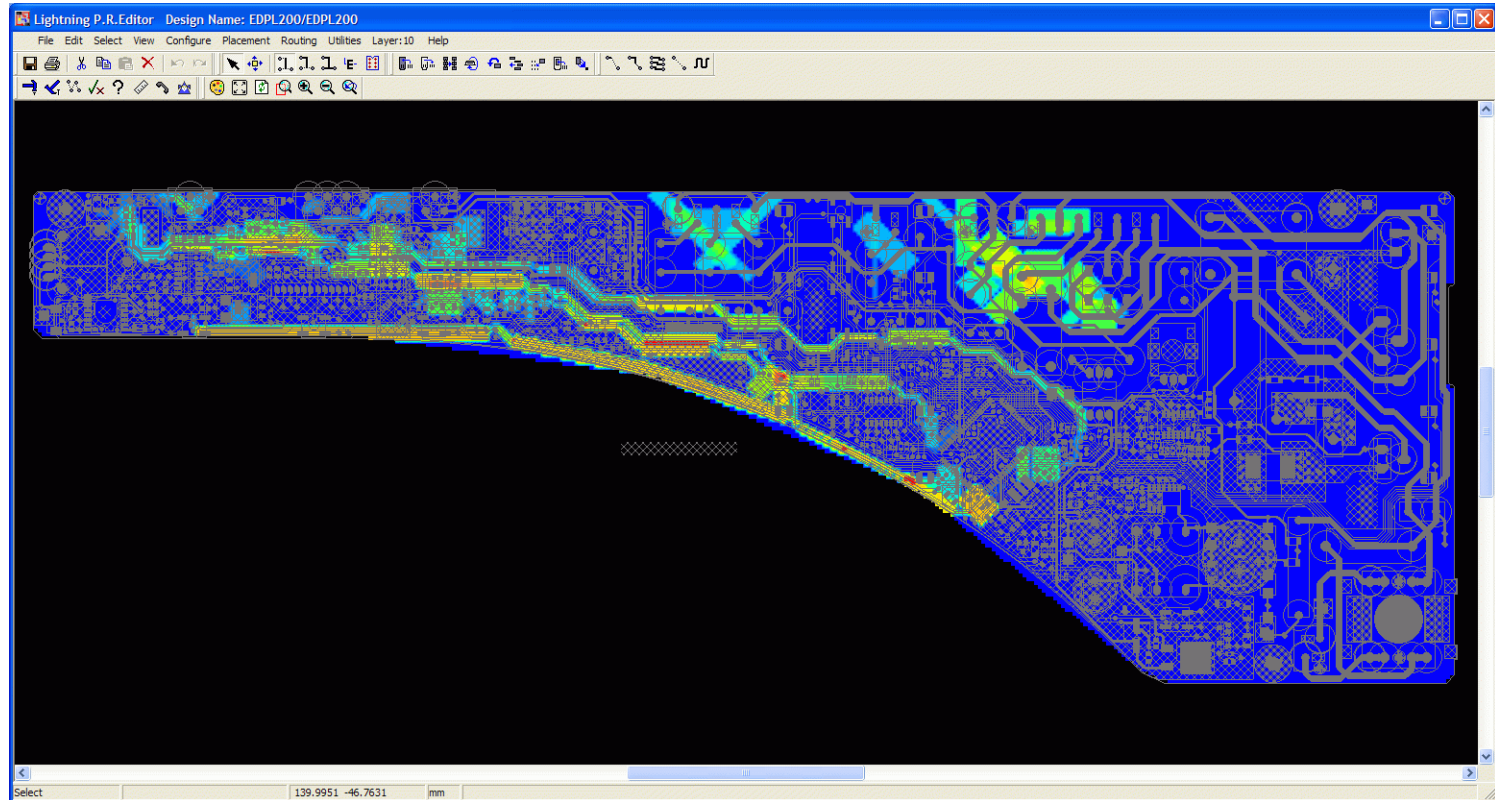
- Caused by parasitic antennas which are built up by:
  - Board to heat-sink coupling
  - Coupling between connectors
  - Board to connector coupling
  - Connector to heat-sink coupling
  - Coupling through cables





# EMC-Mechanismn: Common Mode EMC

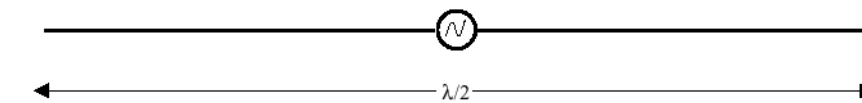
## Common Mode: I/O-Coupling



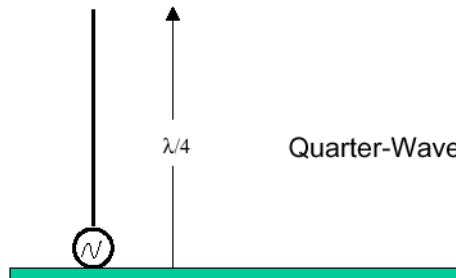
Crosstalk between fast signals to neighbourhood (IO) lines will cause noise voltages visible at the connectors



# Again: Effective Antennas



Half-Wave Dipole ↑

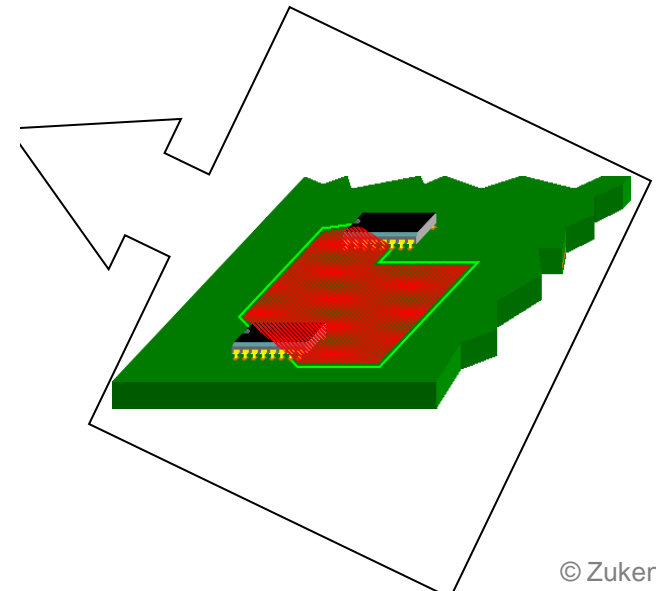
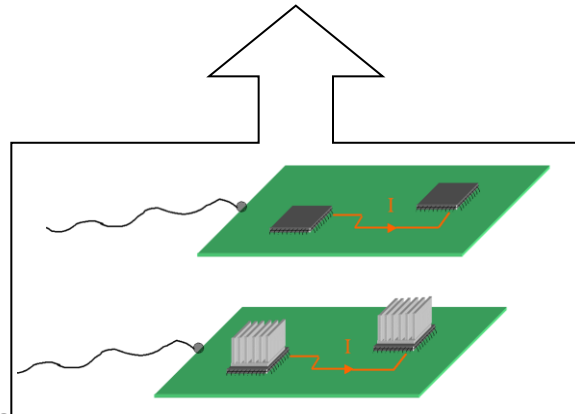
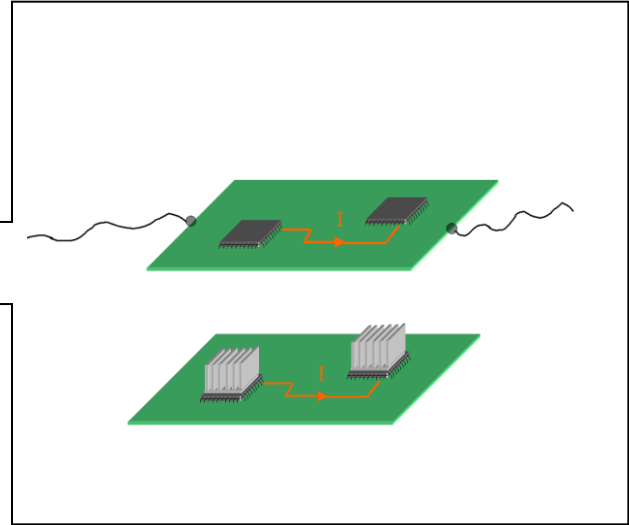


Quarter-Wave Monopole ↑

Electrically Small Loop ↓



- Size
- Two Halves

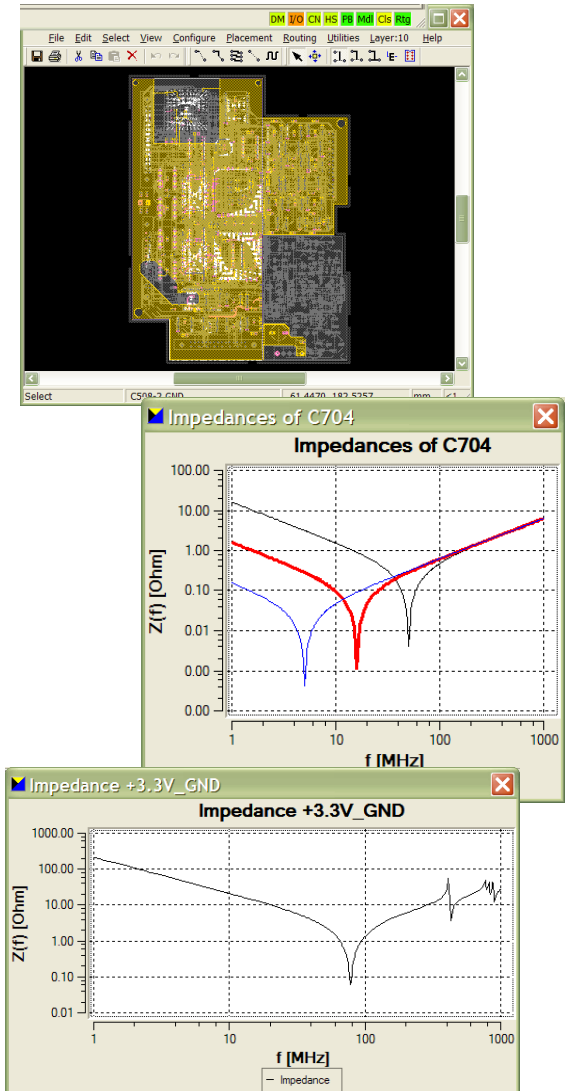




# PI Advance - Power Integrity Analysis

## Capabilities of the Lightning PI Advance Power Integrity Solver

- ☑ Fast method to investigate the quality and efficiency of all supply systems of a PCB:
  - **Detection of:**
    - ✓ Ineffective decaps,
    - ✓ High impedance connection of decaps to power supply system,
    - ✓ Critical input buffers, w.r.t. the power bus noise voltage.
  - **Estimation of:**
    - ✓ Effective capacitance of total power bus,
    - ✓ Total power bus impedance (including self resonances),
    - ✓ Current drawn by each IC,
    - ✓ Power bus noise voltage, and
    - ✓ Radiated electrical field.





# PI Advance: Decoupling Analysis & What If

DeCap potentially not effective ?

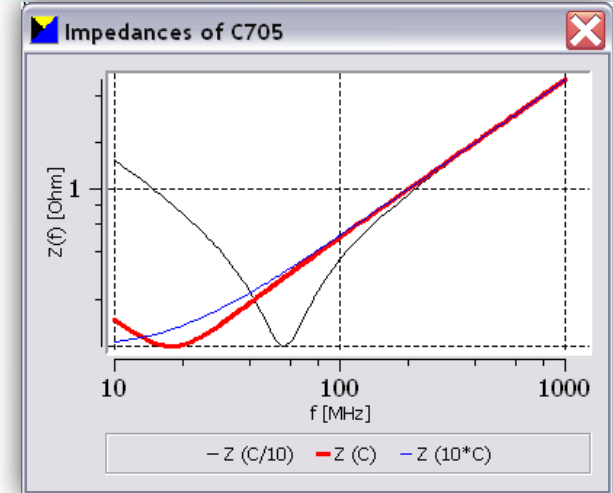
Lightning EMC - routed.rif

File Edit Simulation Window Help

Common JC Decap

Component	Value [nF]	Inductance [nH]	Res. Freq. f <sub>0</sub> [MHz]	Ineffect	Power Bus	SMD	Nearest IC
C610	100.00	1.94	11.42		+3.3V_GND	Yes	U100
C611	100.00	9.41	5.19		+3.3V_GND	Yes	U602
C700	100.00	3.27	8.80		+3.3V_GND	Yes	U400
C701	100.00	1.55	12.80		+3.3V_GND	Yes	U700
C702	100.00	1.56	12.76		+3.3V_GND	Yes	U108
C703	100.00	2.28	10.55		+3.3V_GND	Yes	U404
C704	47000.00	0.80	0.82		+3.3V_GND	Yes	U604
<b>C705</b>	<b>100.00</b>	<b>0.80</b>	<b>17.79</b>		<b>+3.3V_GND</b>	<b>Yes</b>	<b>U902</b>
C706	100.00	1.44	13.26		+3.3V_GND	Yes	U504
C707	100.00	1.69	12.25		+3.3V_GND	Yes	U103
C708	100.00	0.80	17.79		+3.3V_GND	Yes	U500
C709	100.00	0.80	17.79		+3.3V_GND	Yes	U603
C802	220000.00	0.80	0.38		+3.3V_GND	Yes	U106
C803	100.00	0.80	17.79		+3.3V_GND	Yes	U106

DM I/O CN HS PB: Md Gs Rtg



Change Value within Lightning from 470p to 100N → Quick What-If

Lightning EMC - routed.rif - [Classification]

File Edit Simulation Window Help

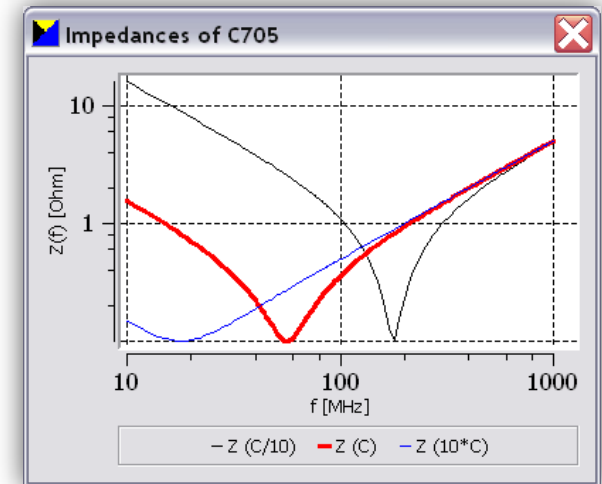
Component Net Supply Power Bus

Component	Name	Part Name	Component Type	Value	Active	# Pins	HeatSink
C702	C702	MCH182F104Z	Decap	100.00	yes	2	no
C703	C703	MCH182F104Z	Decap	100.00	yes	2	no
C704	C704	MSV021C476M	Decap	47000.00	yes	2	no
<b>C705</b>	<b>C705</b>	<b>MCH182F104Z</b>	<b>Decap</b>	<b>100.00</b>	<b>yes</b>	<b>2</b>	<b>no</b>
C706	C706	MCH182F104Z	Decap	100.00	yes	2	no
C707	C707	MCH182F104Z	Decap	100.00	yes	2	no
C708	C708	MCH182F104Z	Decap	100.00	yes	2	no
C709	C709	MCH182F104Z	Decap	100.00	yes	2	no
C710	C710	MCH182F104Z	Capacitor	100.00	yes	2	no
C711	C711	MCH182F104Z	Capacitor	100.00	yes	2	no
C800	C800	UWX1H100MCR1GB	Capacitor	10000.00	yes	2	no
C801	C801	UWX1H100MCR1GB	Capacitor	10000.00	yes	2	no
C802	C802	UUR1V221MNT1GS	Decap	220000.00	yes	2	no
C803	C803	GRMA0F104Z50PT	Decap	100.00	yes	2	no
C804	C804	UUR1H101MNT1GS	Capacitor	47000.00	yes	2	no

Pin Power Bus

Component	Power Bus	C PD I/O [nF]	C PD Core [nF]	# Core Pins	Core Frequency [MHz]	ESR [Ohm]	ESL [nH]	C in [nF]
C705	+3.3V_GND					0.10	0.10	100.00

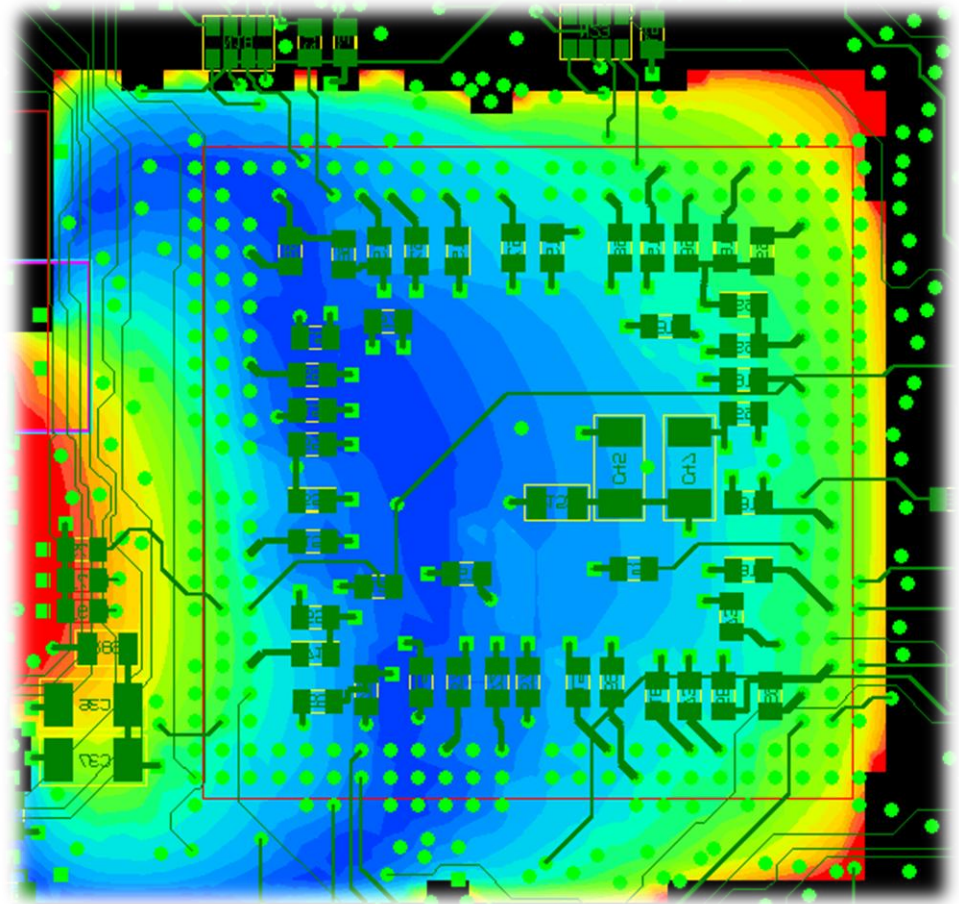
DM I/O CN HS PB: Md Gs Rtg





# PI Advance: Decoupling Effectiveness over frequency for Copper Power Areas

- Impedance distribution at target frequencies show impact of decoupling capacitors
- Indicate quality of placement location, value and connection inductance
- Placement or connection can be changed on the fly in P.R.Editor for what if capabilities

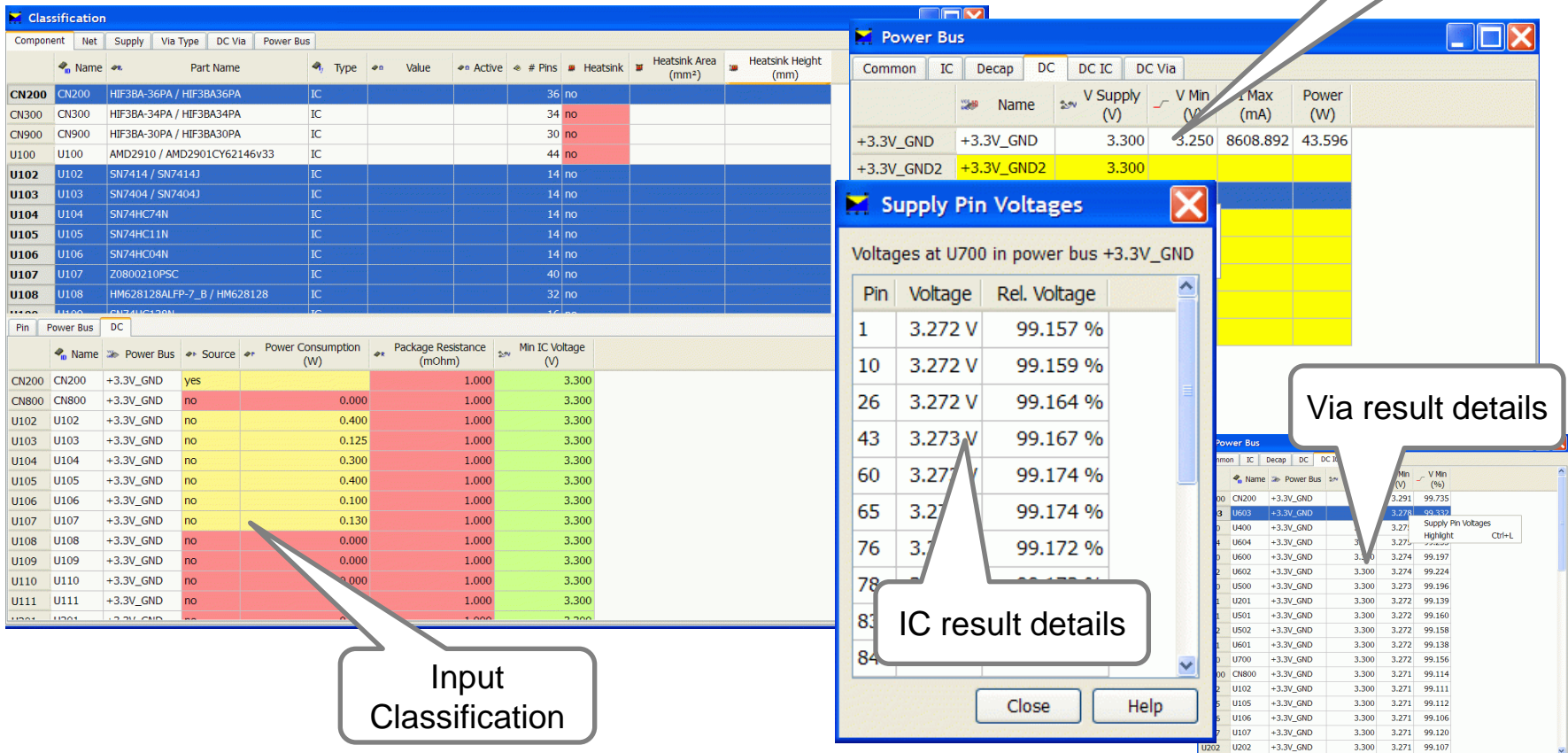




# Lightning PIA: DC Power Integrity

## DC-Analysis of supply systems

- Table driven DC-Analysis
- Results for supply system / ICs / Vias in separate tables



**Classification**

Component	Net	Supply	Via Type	DC Via	Power Bus			
Name	Part Name	Type	Value	Active	# Pins	Heatsink	Heatsink Area (mm <sup>2</sup> )	Heatsink Height (mm)
CN200	HIF3BA-36PA / HIF3BA36PA	IC			36	no		
CN300	HIF3BA-34PA / HIF3BA34PA	IC			34	no		
CN900	HIF3BA-30PA / HIF3BA30PA	IC			30	no		
U100	AMD2910 / AMD2901CY62146V33	IC			44	no		
U102	SN7414 / SN7414J	IC			14	no		
U103	SN7404 / SN7404J	IC			14	no		
U104	SN74HC74N	IC			14	no		
U105	SN74HC11N	IC			14	no		
U106	SN74HC04N	IC			14	no		
U107	Z0800210PSC	IC			40	no		
U108	HM628128ALFP-7_B / HM628128	IC			32	no		
U109	U109	IC			16	no		

**Power Consumption**

Pin	Power Bus	DC	Name	Power Bus	Source	Power Consumption (W)	Package Resistance (mOhm)	Min IC Voltage (V)
CN200	CN200	+3.3V_GND	yes				1.000	3.300
CN800	CN800	+3.3V_GND	no			0.000	1.000	3.300
U102	U102	+3.3V_GND	no			0.400	1.000	3.300
U103	U103	+3.3V_GND	no			0.125	1.000	3.300
U104	U104	+3.3V_GND	no			0.300	1.000	3.300
U105	U105	+3.3V_GND	no			0.400	1.000	3.300
U106	U106	+3.3V_GND	no			0.100	1.000	3.300
U107	U107	+3.3V_GND	no			0.130	1.000	3.300
U108	U108	+3.3V_GND	no			0.000	1.000	3.300
U109	U109	+3.3V_GND	no			0.000	1.000	3.300
U110	U110	+3.3V_GND	no			0.000	1.000	3.300
U111	U111	+3.3V_GND	no			0.000	1.000	3.300

**Power Bus**

Common	IC	Decap	DC	DC IC	DC Via
Name	V Supply (V)	V Min (V)	I Max (mA)	Power (W)	
+3.3V_GND	+3.3V_GND	3.300	3.250	8608.892	43.596
+3.3V_GND2	+3.3V_GND2	3.300			

**Supply Pin Voltages**

Voltages at U700 in power bus +3.3V\_GND

Pin	Voltage	Rel. Voltage
1	3.272 V	99.157 %
10	3.272 V	99.159 %
26	3.272 V	99.164 %
43	3.273 V	99.167 %
60	3.272 V	99.174 %
65	3.272 V	99.174 %
76	3.272 V	99.172 %

**Via result details**

Name	Power Bus	V Min (V)	V Min (%)
CN200	+3.3V_GND	3.291	99.735
U603	+3.3V_GND	3.278	99.332
U400	+3.3V_GND	3.271	99.111
U604	+3.3V_GND	3.271	99.111
U600	+3.3V_GND	3.271	99.111
U602	+3.3V_GND	3.271	99.111
U500	+3.3V_GND	3.271	99.111
U201	+3.3V_GND	3.271	99.111
U501	+3.3V_GND	3.271	99.111
U502	+3.3V_GND	3.271	99.111
U601	+3.3V_GND	3.271	99.111
U700	+3.3V_GND	3.271	99.111
CN800	+3.3V_GND	3.271	99.111
U102	+3.3V_GND	3.271	99.111
U105	+3.3V_GND	3.271	99.111
U106	+3.3V_GND	3.271	99.111
U107	+3.3V_GND	3.271	99.111
U202	+3.3V_GND	3.271	99.111

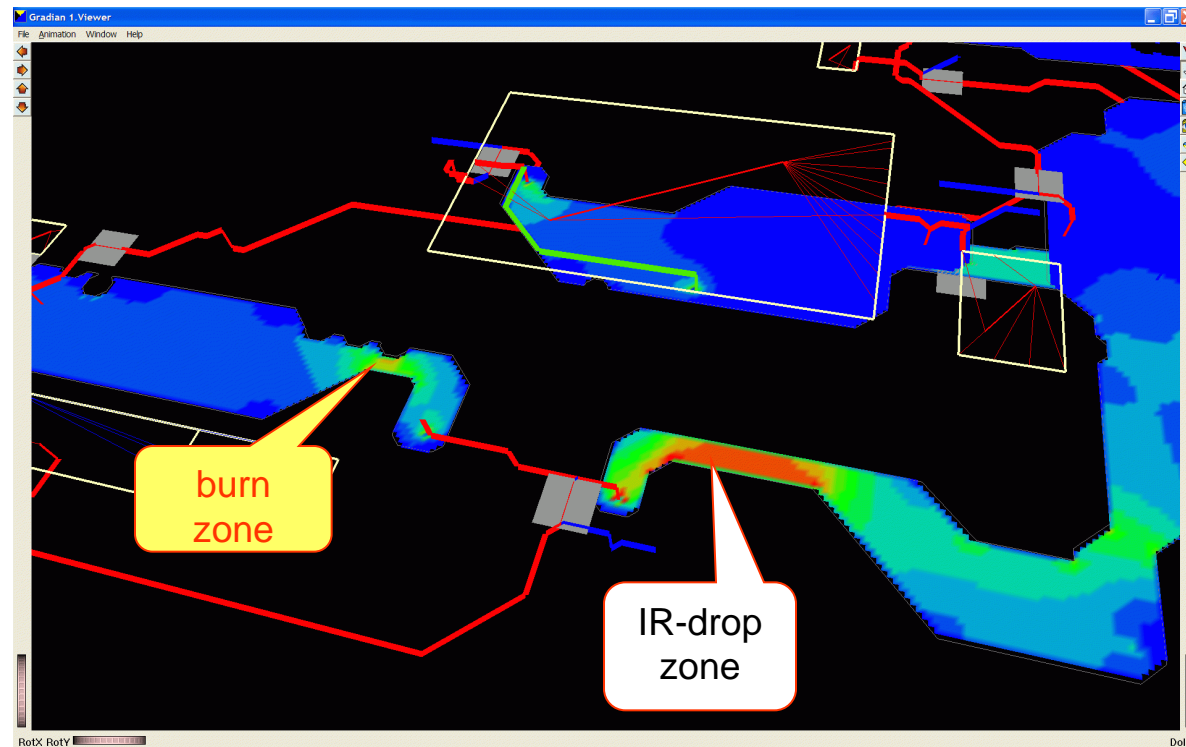
**IC result details**

Close Help



# Lightning PIA: DC Analysis

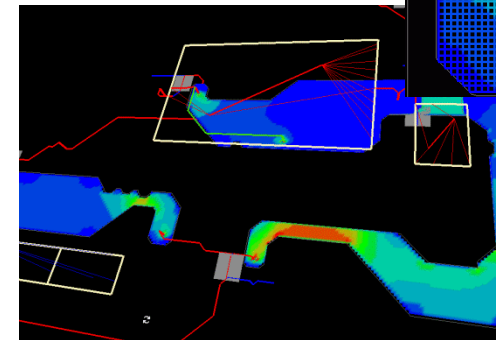
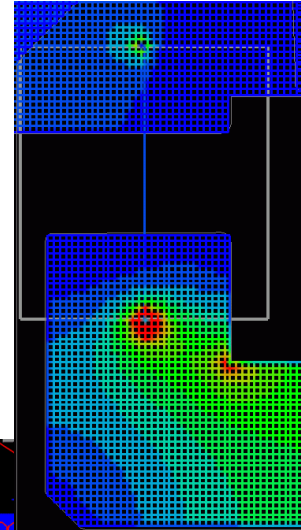
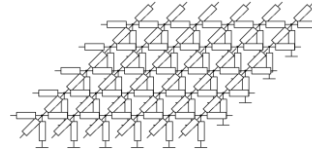
- DC solver allows analysis of DC Current Distribution and IR-Voltage drops within PCB Supply nets
  - High Current Nets as well
  - Detection of potential trouble areas in the Layout
  - Avoiding thermal problems and Power Supply problems





# PI Advance DC Analysis

- Analysis is done highly accurate by numerical solution  
→ R-Cells Grid based approach
- Analysis is done very efficiently  
→ large electrical system is divided into smaller portions
- Results are visualized graphically in 3D
- Tabular results given in spreadsheet
  - Can easily be compared with given limits



Power Bus

Common	IC	Decap	DC	DC IC	DC Via
Component	Power Bus	V Supply [V]	V_Min [V]	rel. V_Min [%]	
CN501	CN501	SW+3.3V_EURO_GND_AUDIO	3.300	3.300	100.000
IC106	IC106	SW+3.3V_EURO_GND_AUDIO	3.300	3.199	96.930
IC103	IC103	SW+3.3V_EURO_GND_AUDIO	3.300	3.197	96.888
IC102	IC102	SW+3.3V_EURO_GND_AUDIO	3.300	3.197	96.885
IC104	IC104	SW+3.3V_EURO_GND_AUDIO	3.300	3.196	96.846
CN107	CN107	SW+3.3V_EURO_GND_AUDIO	3.300	3.181	96.400
CN106	CN106	SW+3.3V_EURO_GND_AUDIO	3.300	3.181	96.400
IC403	IC403	AU+11V_EURO_GND_AUDIO	11.000		
IC402	IC402	AU+11V_EURO_GND_AUDIO	11.000		

Per net and IC

IC per Pin

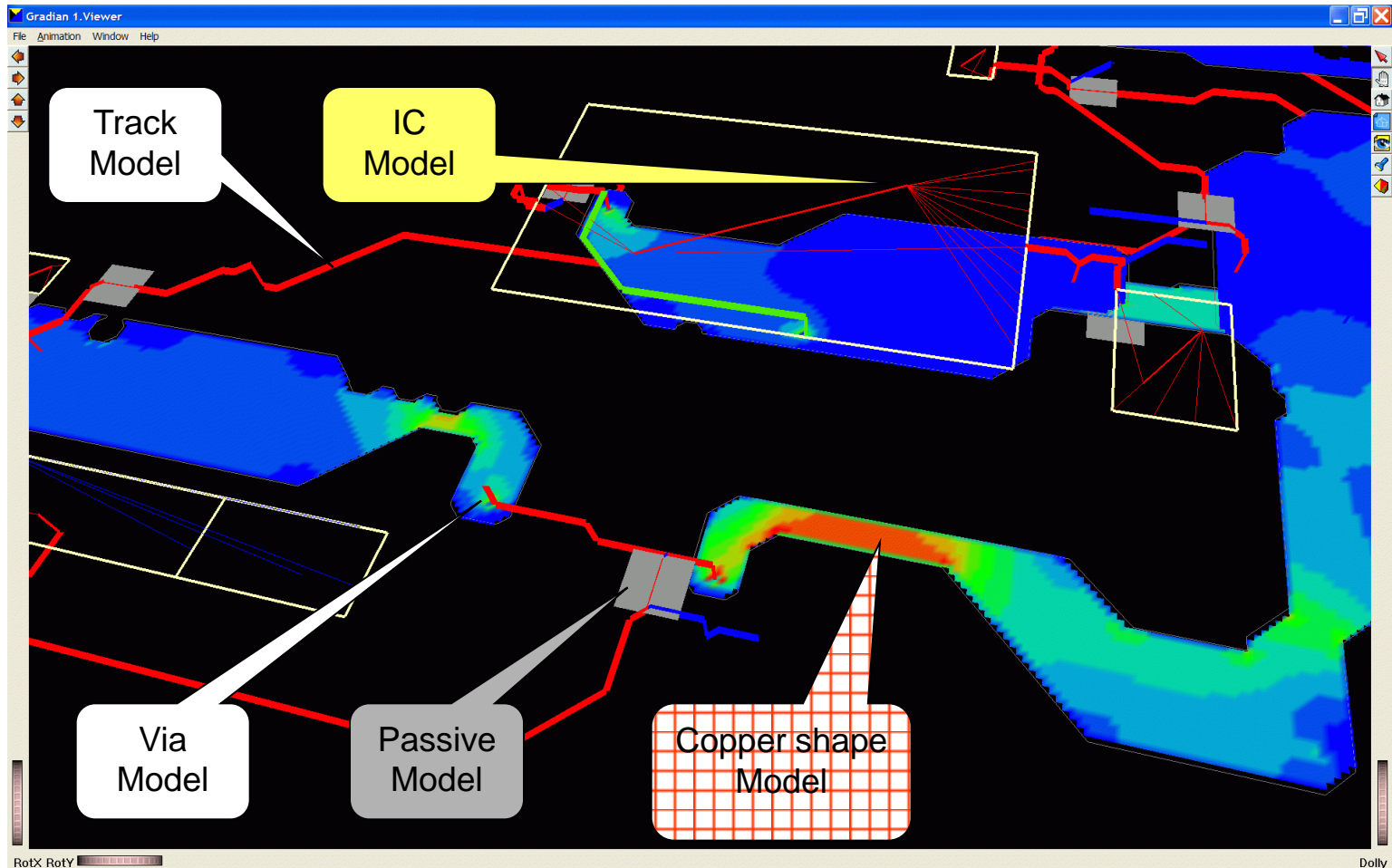
Pin Name	DC Voltage
49	3.196 V
43	3.196 V
27	3.196 V
14	3.196 V
9	3.196 V
3	3.196 V
1	3.196 V

Per IC pin



# PI Advance DC Analysis




- Model Details





# Sample: Investigation of critical Power Bus

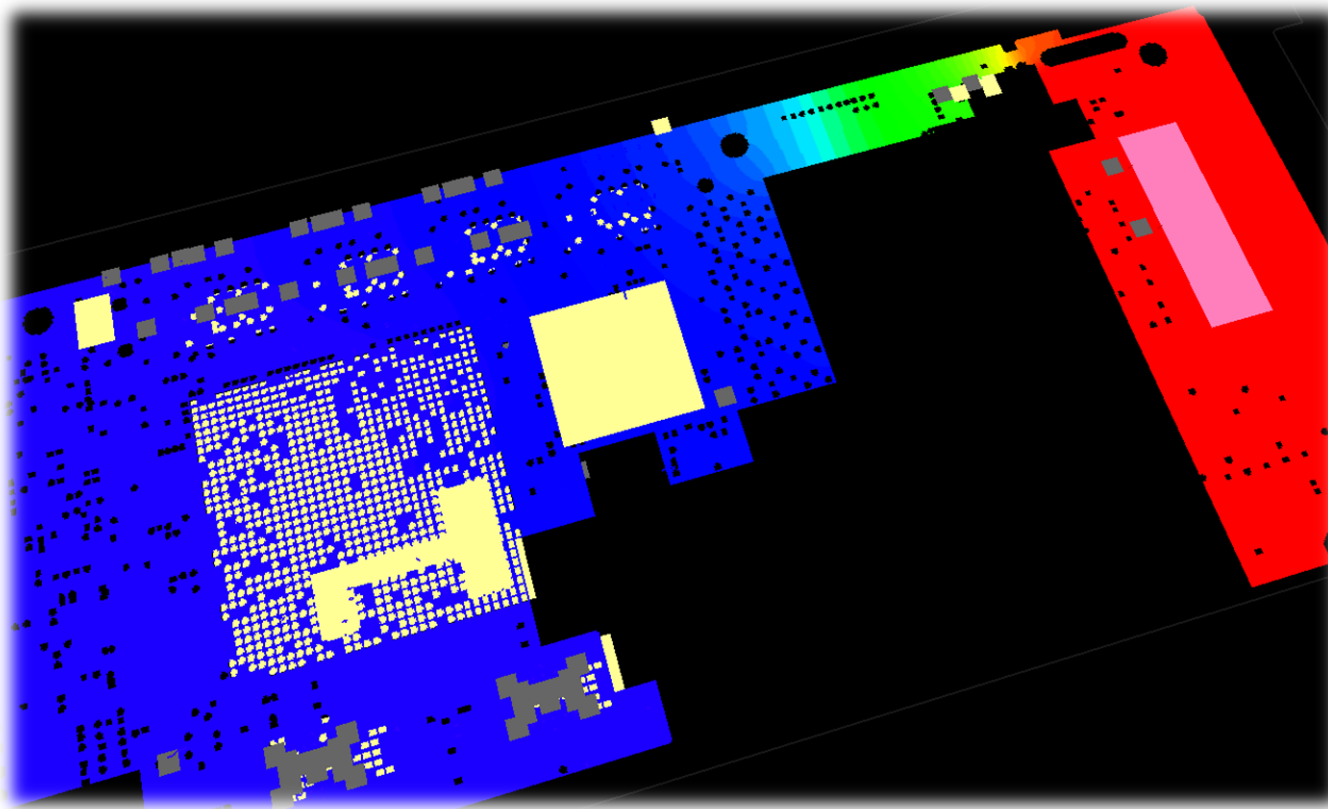
## +1,8V-GND - DC Simulation

Common	IC	Decap	DC	DC IC	DC Via				
			Name		V Supply (mV)		V Min (mV)	I Max (mA)	Power (W)
+1,8V_GND			+1,8V_GND		1800.00		1768.43	2183.24	3.93

Grid Size

Min Grid Size: 50.000   $\mu\text{m}$

Max Grid Size: 200.000   $\mu\text{m}$

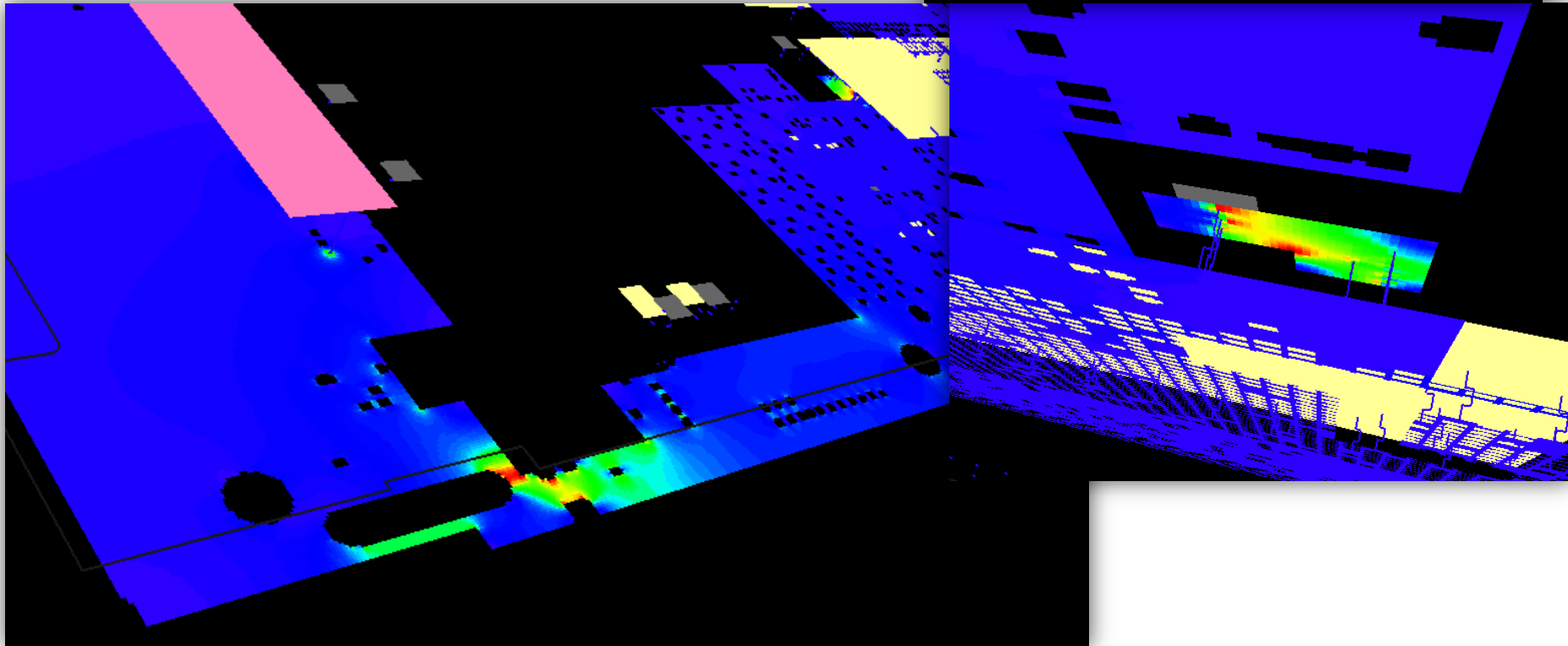
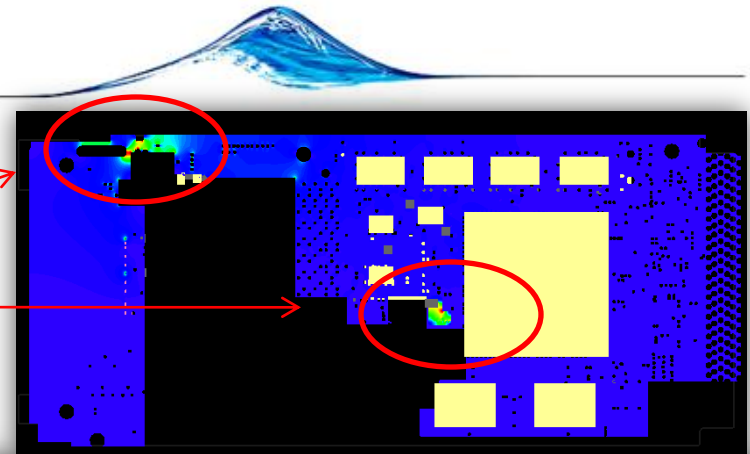


**Voltage Distribution (V):**  
Max. Voltage Drop = 32mV



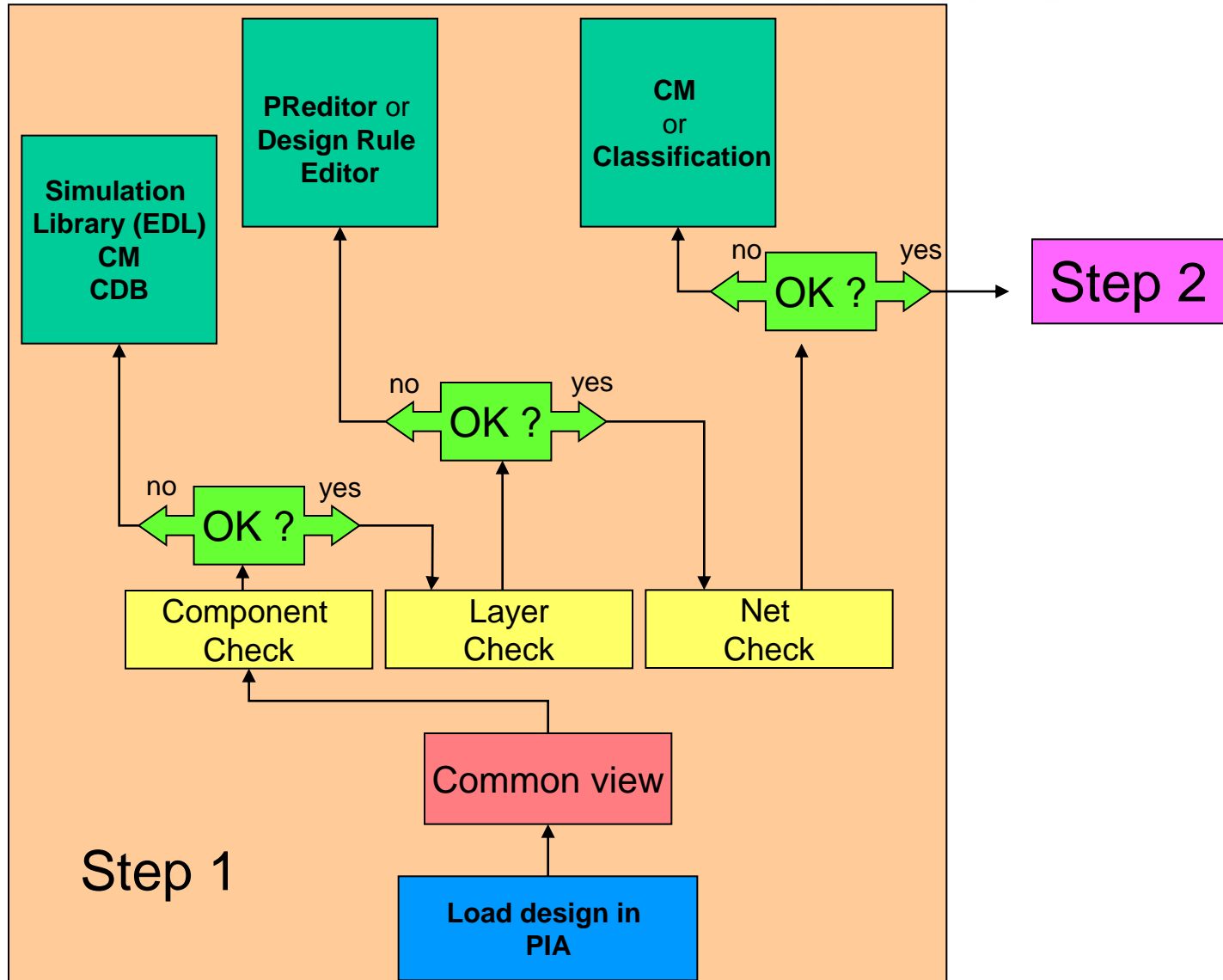
# Investigation of critical Power Bus: +1,8V-GND - DC Simulation

**Current Density (J) → 2 Current hot-spots**



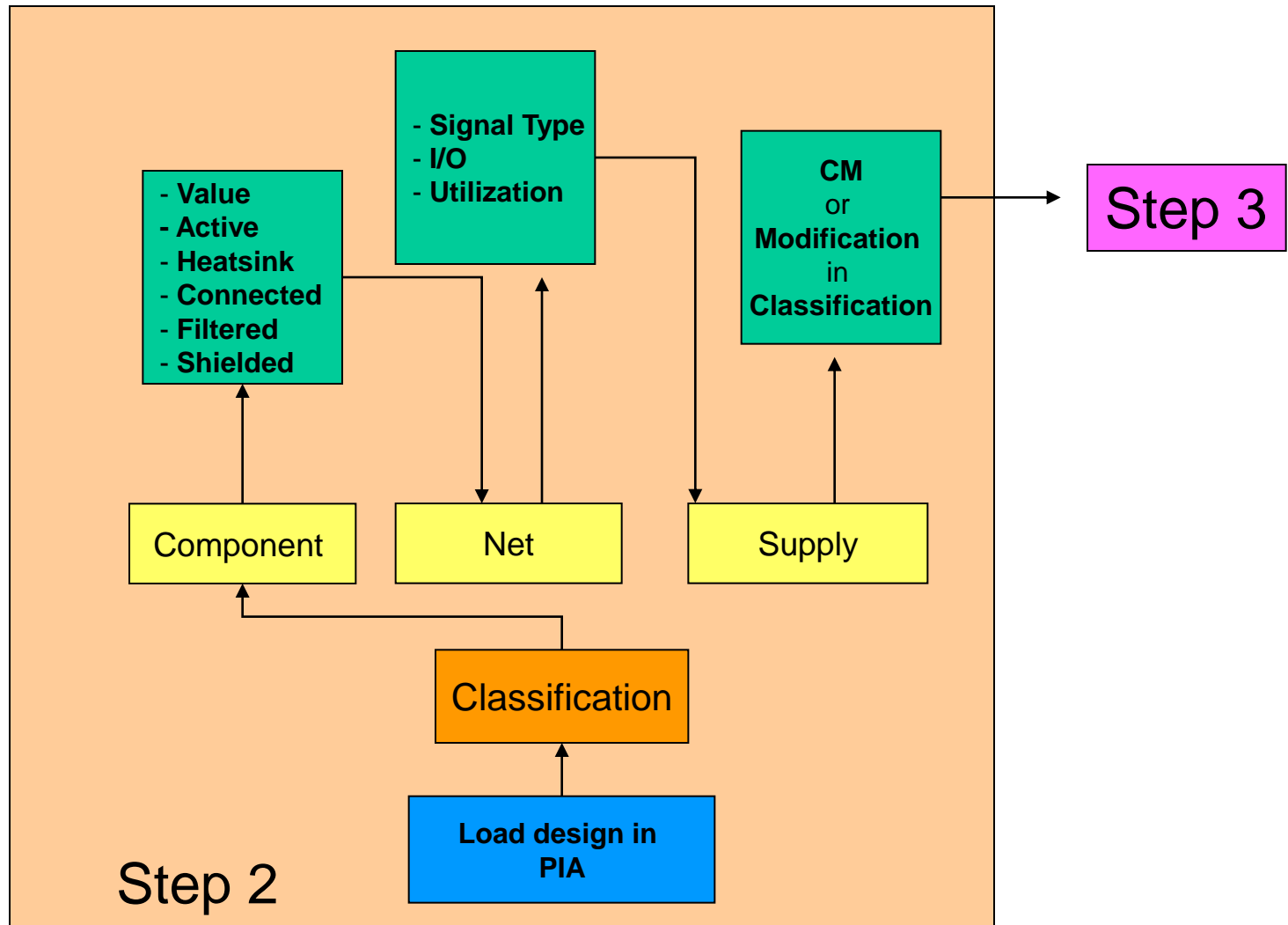


# PIA Working Flow (1 of 3)



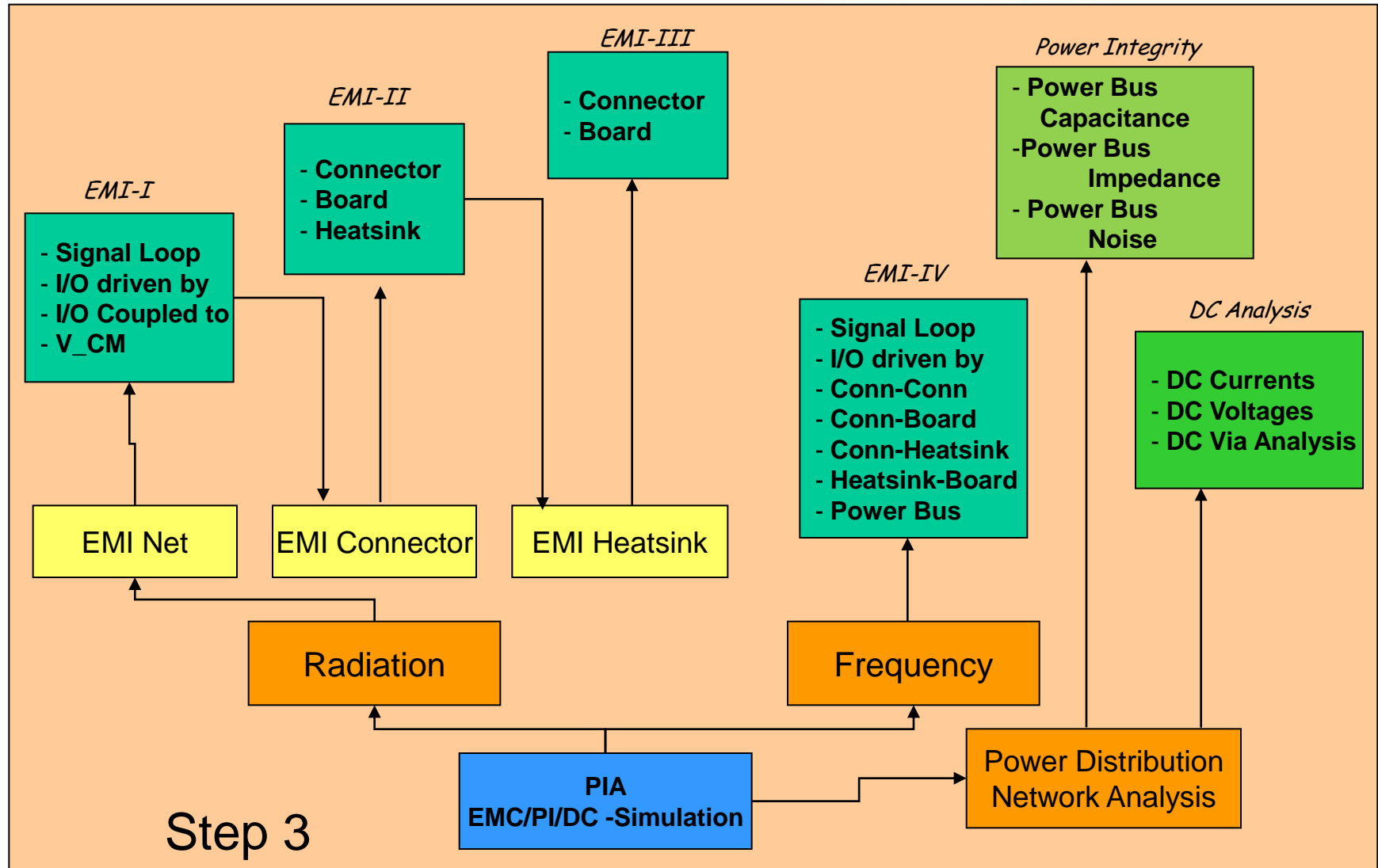


## PIA Working Flow (2 of 3)





# PIA Working Flow (3 of 3)





# Library/Attribute Information for PIA

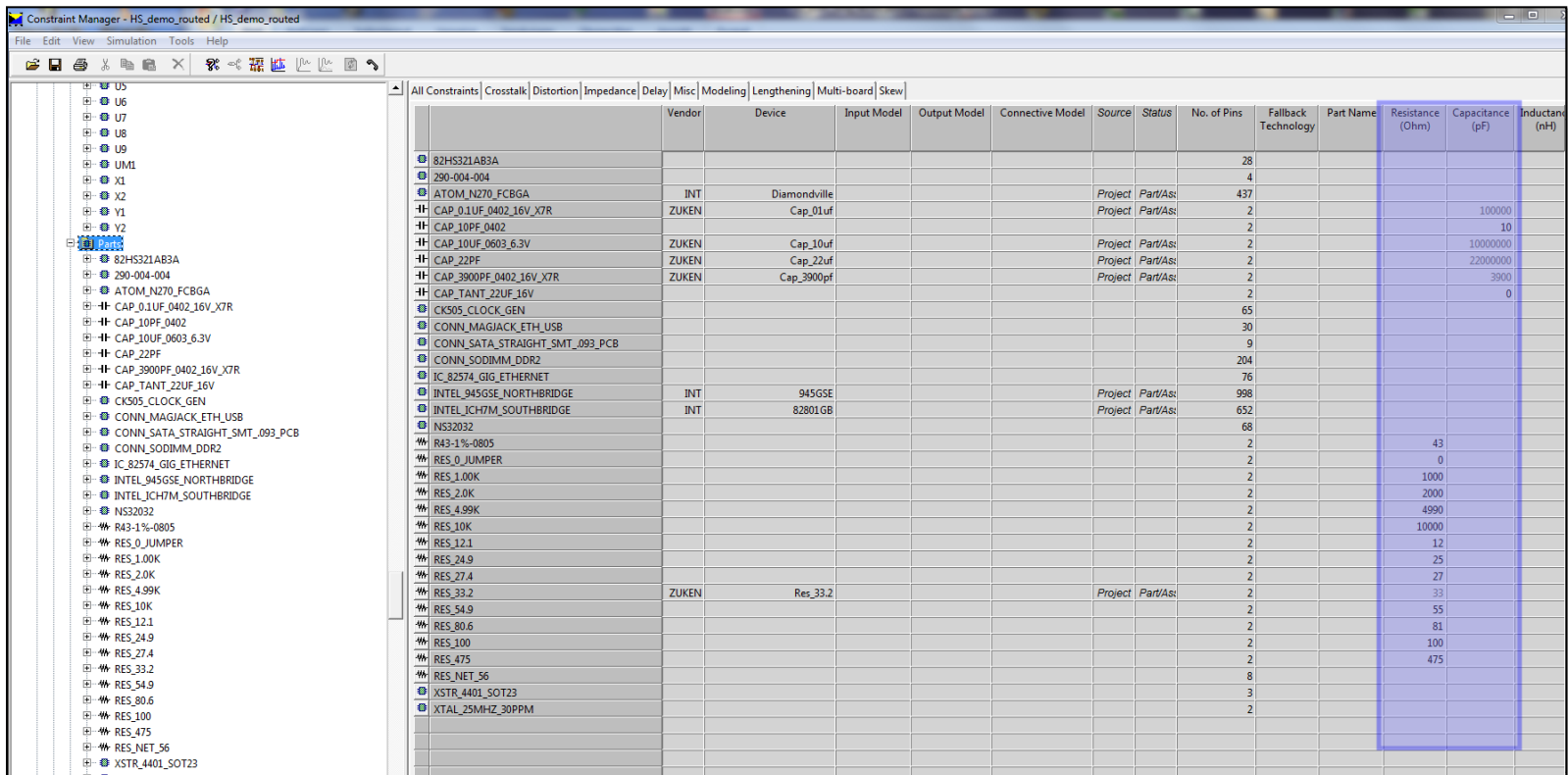
- PIA needs some information (of course) to work properly (but no special models nor special data setup is necessary) – even better, in a high-speed or SI flow it should work smoothly.
- It needs information (like a human expert), otherwise its blindfolded (like a human expert will be too).
- It does not need special models, but if presents uses information from IBIS models assigned
- First of all, it needs copper (airlines are not antennas, templates have no capacitance) – however, the board must NOT be completely routed !
- The user has to a certain extend interact with the software (→ Classification), this is a mandatory step !
- With respect to data, PI Advance needs to know:
  - Layer stack (not a surprise, correct ?)
  - Materials (conductivity)
  - Device types (RES/CAP/IND), as well ICs and Connectors (for EMI analysis)
  - Heatsinks (for EMC analysis)
  - Values of discrete components
  - Power/GND Pins of devices (connection to power supply systems)
  - ESL/ESR values of DeCaps (for PI AC analysis)
  - Source/Sink Current Path and Power Dissipation of ICs(for PI DC analysis)



# Exercise 1: Check Design Data for PIA

## Steps:


1. Launch Pred-HS on design *hs\_demo\_routed*
2. Select Parts in the CM Tree View
3. Switch to Modelling TAB
4. Compare the entries with those in the picture, **discuss** differences and impact of those (ICs but as well resistors and capacitors) **with your trainer.** (we will fix that later in an exercise and with provided data set)

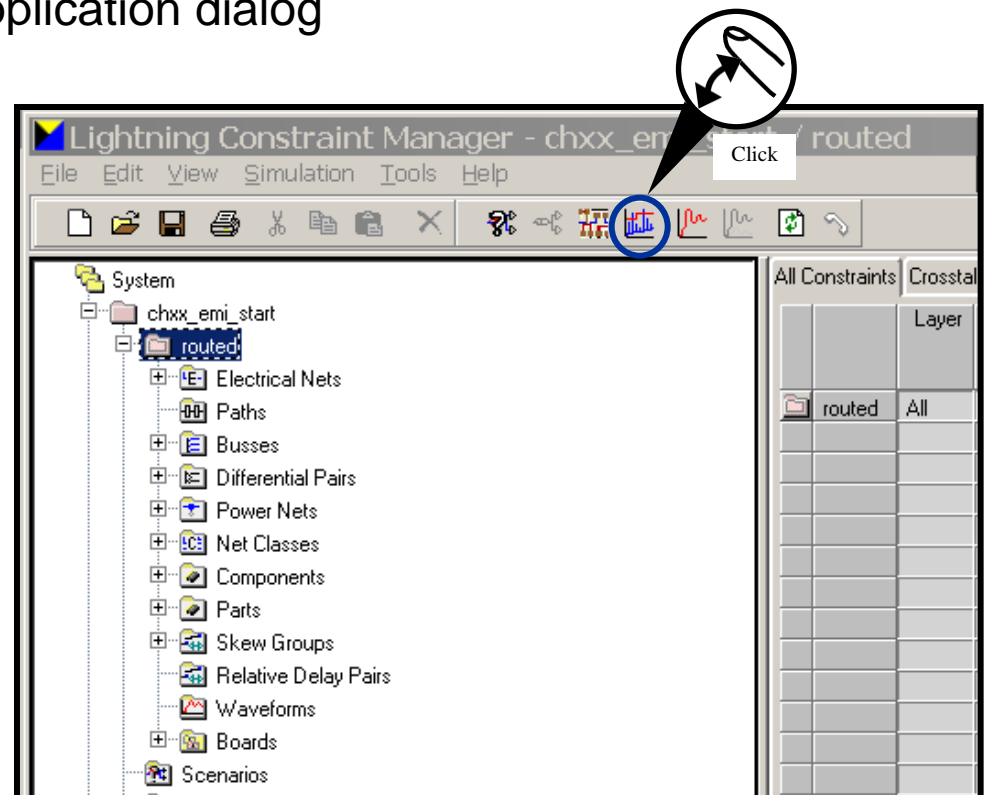


	Vendor	Device	Input Model	Output Model	Connective Model	Source	Status	No. of Pins	Fallback Technology	Part Name	Resistance (Ohm)	Capacitance (pF)	Inductance (nH)
82HS321AB3A								28					
290-004-004								4					
ATOM_N270_FCBGA	INT	Diamondville				Project	Part/As:	437					
CAP_0.1UF_0402_16V_X7R	ZUKEN	Cap_01uf				Project	Part/As:	2				100000	
CAP_10PF_0402								2				10	
CAP_10UF_0603_6.3V	ZUKEN	Cap_10uf				Project	Part/As:	2				10000000	
CAP_22PF	ZUKEN	Cap_22uf				Project	Part/As:	2				22000000	
CAP_3900PF_0402_16V_X7R	ZUKEN	Cap_3900pf				Project	Part/As:	2				3900	
CAP_TANT_22UF_16V								2				0	
CKS05_CLOCK_GEN								65					
CONN_MAGJACK_ETH_USB								30					
CONN_SATA_STRAIGHT_SMT_093_PCB								9					
CONN_SODIMM_DDR2								204					
IC_82574_GIG_ETHERNET								76					
INTEL_945GSE_NORTHBRIDGE	INT	945GSE				Project	Part/As:	998					
INTEL_ICH7M_SOUTHBRIDGE	INT	82801GB				Project	Part/As:	652					
NS32032								68					
R43-1%-0805								2			43		
RES_0_JUMPER								2			0		
RES_1.00K								2			1000		
RES_2.0K								2			2000		
RES_4.99K								2			4990		
RES_10K								2			10000		
RES_12.1								2			12		
RES_24.9								2			25		
RES_27.4								2			27		
RES_33.2	ZUKEN	Res_33.2				Project	Part/As:	2			33		
RES_54.9								2			55		
RES_80.6								2			81		
RES_100								2			100		
RES_475								2			475		
RES_NET_56								8					
XSTR_4401_SOT23								3					
XTAL_25MHZ_30PPM								2					



# How to launch PI-Advance


- From the software bundling point of view PIA is an add-on option to PReditor HS (mandatory), but not license wise related to SI-Verify
- PI-Advance is to be launched from CM using the  icon (or Tools-PIA)
- PIA Icon gets active (only) when a license is present !
- PIA will start up as separate application dialog

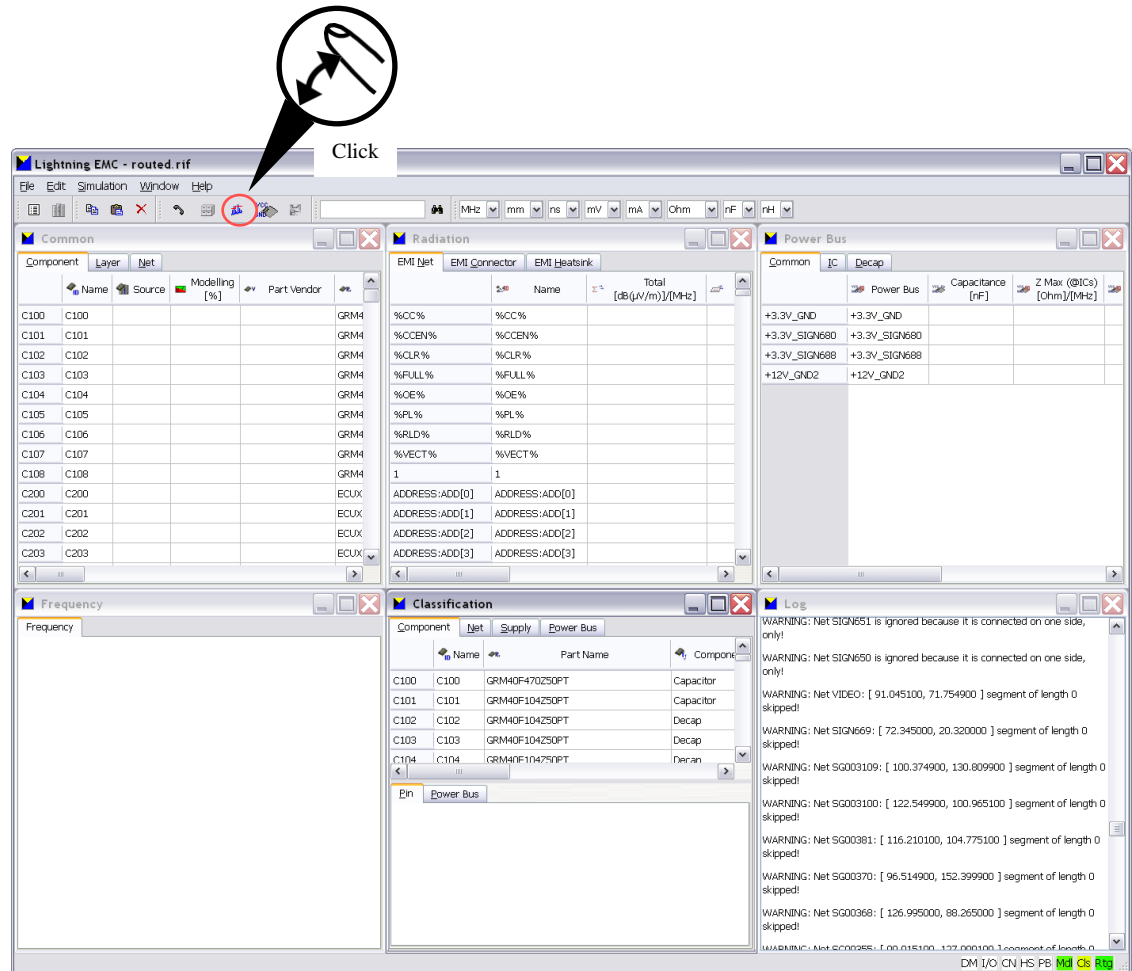




# Exercise 2: Launch PIA & perform a EMI Analysis

## Steps:

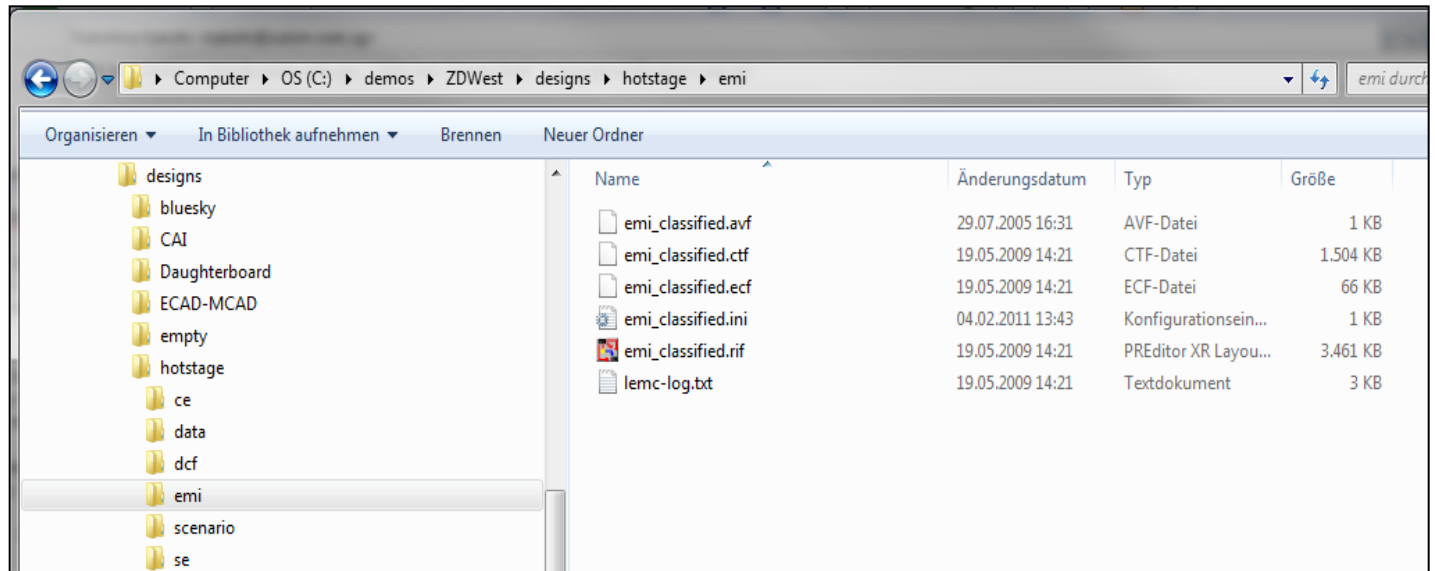
1. Launch PI Advance on design *hs\_demo\_routed*
2. Run EMC Analysis 
3. Raise Result Window (Radiation)
4. Inspect the various GUI columns
5. Why some columns in the various results window are empty, others are filled ?





# PI-Advance Information: Data Files

- Some technical details behind
  - PI Advance reads **CTF** and **RIF** files from <design>\hotstage\emi directory
  - As PI Advance needs the newest RIF format , PI Advance keeps a clone of the design RIF and CTF under <design>\hotstage\emi directory
    - Stored as well is classification data (.ecf) and options (.INI)
    - These files are stored in XML or plain ASCII


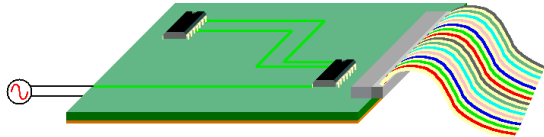




# PI-Advance Information:

## SI-Simulation vs. PIA EMC Analysis



	SI-Simulation (LT/SIV)	PI Advance (EMC)
Function	<p>Considers the Signal Quality (Signal Integrity) .</p> <p>Means the quality of signals which arrive at the receiver. (Reflection, Crosstalk, Timing).</p>	<p>Analyses the various Radiation effects on PCBs.</p> <p>→ Which enets could be responsible (in worst case) for radiation.</p>
Typical model	<p>Driver-TL-Receiver</p> 	<p>Driver-TL-Receiver-current + current return path (+ IO-Lines + connectors) → System</p> 
Results	<p>Very accurate.</p> <p>The simulation results can be compared against measurement.</p>	<p>It shows where the problems are (could be).</p> <p>The results are not matchable (comparable) to the results from the measurement (chamber) but...</p>



# PI-Advance Information:

## SI-Simulation vs. PIA EMC Analysis



	SI-Simulation (LT/SIV)	PI Advance (EMC)
Process (relevant for simulation)	<p>scs.exe (interactive simulation)</p> <p>scs.exe (batch simulator)</p> <p>impulse.exe (Library)</p> <p>Client Server architecture, if needed, SCS will restart automatically</p>	<p>engineer.exe engineer_solver.exe</p> <p>Only 1 engineer can run properly on a system. (On hang-up, user may have to restart the system (because new bmsmain process is needed → sweeper))</p> <p>Needs/uses impulse.exe as well !</p>
Required data	CTF	<p>RIF + CTF, to be found in the directory: &lt;design&gt;\hotstage\emi</p> <p>Classification file .ECF</p>
Results are computed by	<p>Field Solver + Simulation Engine (Telegrapher Equation Solver)</p> <p>Time Domain !</p>	<p>Fast UMR (University of Missouri Rolla) EMC algorithms for full PCB EMC simulation, developed by UMR EMC Expert System consortium.</p> <p>Frequency Domain !</p>



# PI Advance GUI

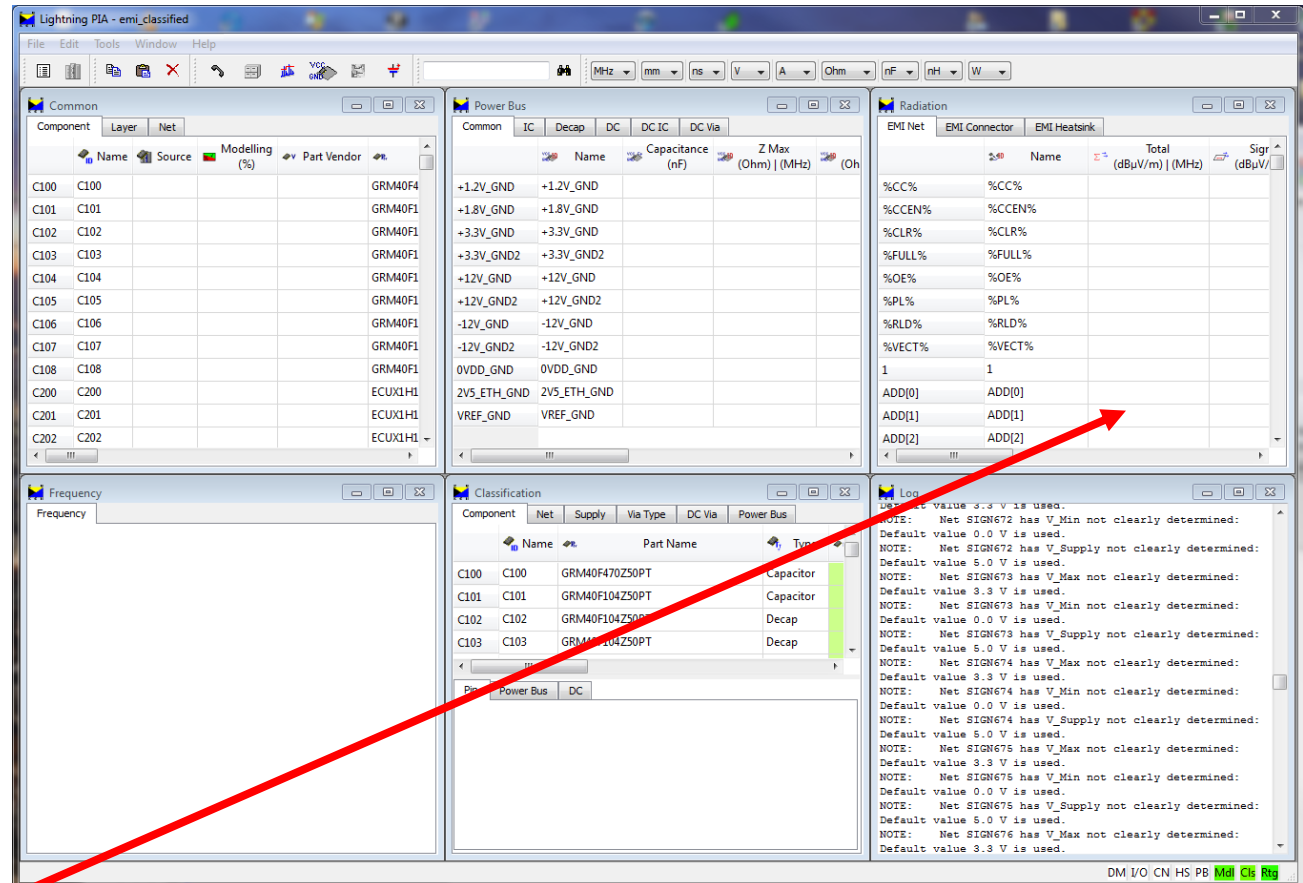


When PI Advance is launched (after CM has written the design data), the GUI is populated with the current design data

→ Some pre-processing is done on these data

→ Only Common (and classification if data is there) cells are filled.

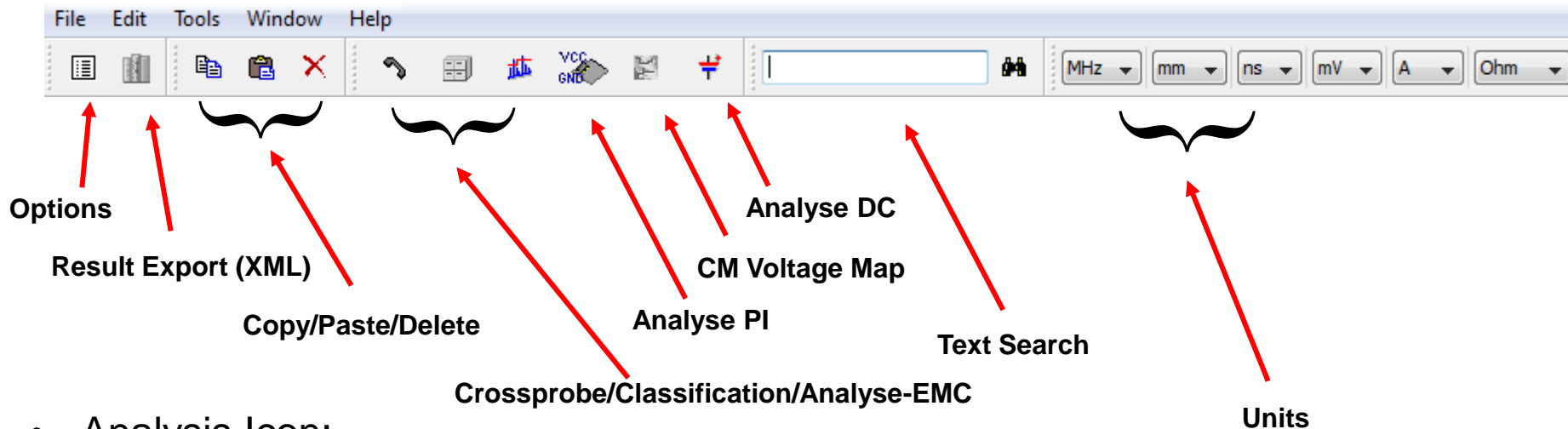
There are no results available then !





# PI Advance GUI Issues (1 of 5)

## • Top Menu+Icon Bar

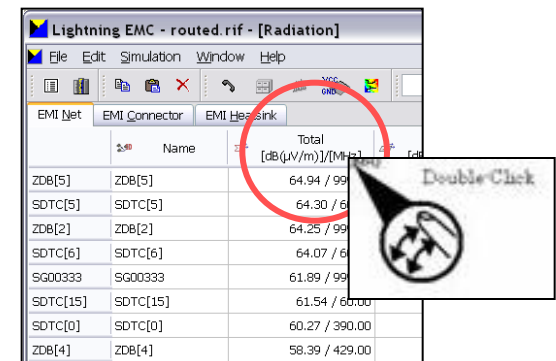


## • Analysis Icon:

- **Sensitive** if no results are there, **insensitive** after analysis
- Becomes sensitive again if settings or data have changed (results are discarded then)

## • All columns can be sorted (click on column header):

- Ascending
- Descending



Lightning EMC - routed.rif - [Radiation]

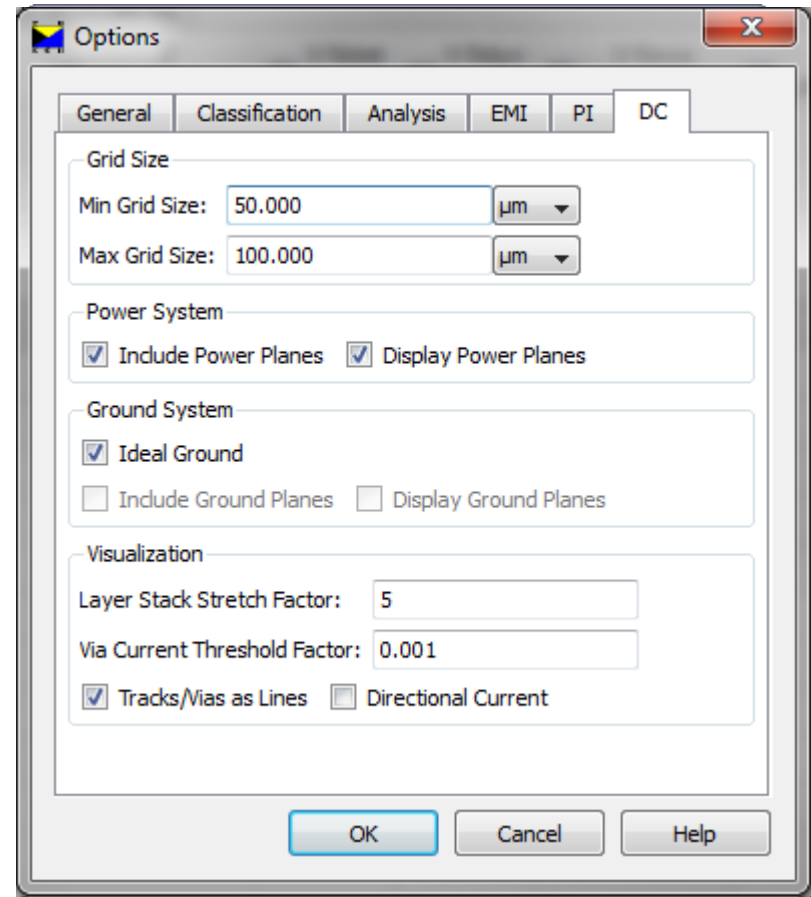
EMI Net	EMI Connector	EMI Hssink	Total [dB(μV/m)]/[MHz]
ZDB[5]	ZDB[5]		64.94 / 99
SDTC[5]	SDTC[5]		64.30 / 6
ZDB[2]	ZDB[2]		64.25 / 99
SDTC[6]	SDTC[6]		64.07 / 6
SG00333	SG00333		61.89 / 99
SDTC[15]	SDTC[15]		61.54 / 6000
SDTC[0]	SDTC[0]		60.27 / 390.00
ZDB[4]	ZDB[4]		58.39 / 429.00



# PI Advance GUI Issues (2 of 5)

## Options:

- General: Decimal points & axis control
- Classification
- Analysis Settings
- EMI: Change antenna distance for far field analysis ( $\geq 3\text{m}$ )
- PI: Effective Series Resistance (ESR) and Effective Series Inductance (ESL) defaults, analysis settings (RLC grid size and grid size relaxation level)
- DC: Grid Size settings, Power/Ground system settings and visualization issues

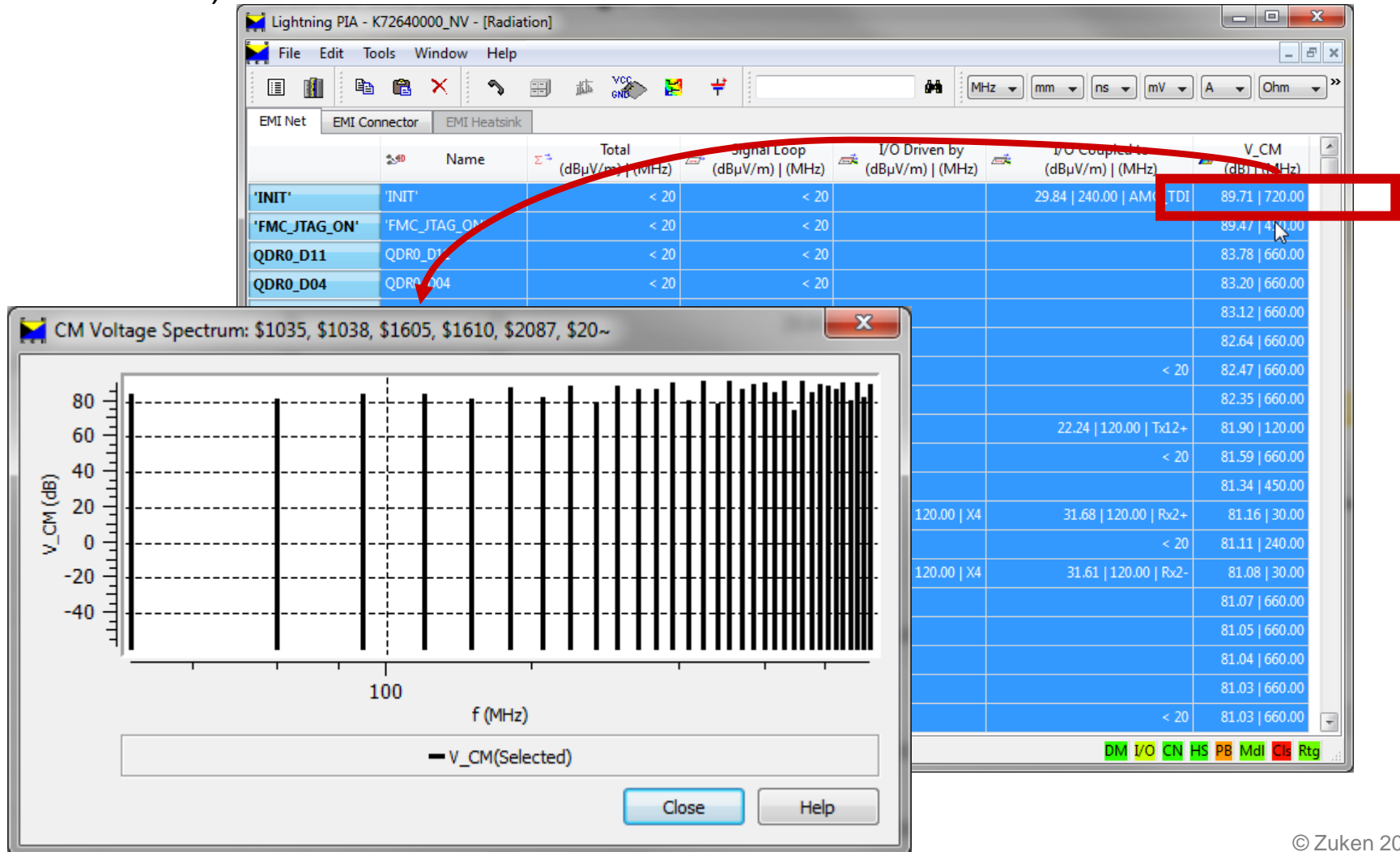




# PI Advance GUI Issues (3 of 5)

Additional information in most table cells (double click of right mouse button RMB)

RMB





## PI Advance GUI Issues (4 of 5)

### Status Bar (lower right of PI-Advance):

The first 5 indicators show green, yellow, or red levels of emissions for a specific EMC effect. These change their status when a given, user-definable threshold is passed. The thresholds are given in dB( $\mu$ V/m).

- **DM:** Differential mode emission
- **I/O:** Emission due to I/O-coupling
- **CN:** Cables, attached at connectors act as antenna for current driven common mode emission.
- **HS:** Heatsinks, act as antenna for current driven common mode emission.
- **PB:** PowerBus noise caused emissions.

The last three indicators have a continuous color between red and green depending on the percentage of:

- **Mdl:** I/O buffer models available at IC pins
- **Cls:** Classification settings are not set to default for: Net type, Clock frequency, Rise- and Fall times
- **Rtg:** Routing completion of the non-supply nets.



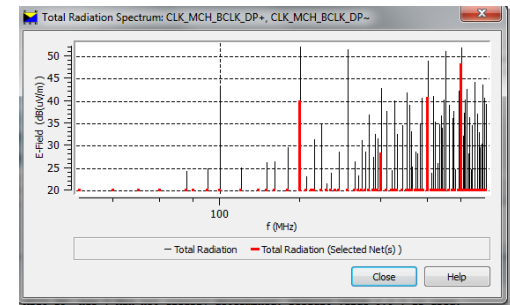


# PI Advance GUI Issues (5 of 5)

## Result/Plot Windows (Spectrum, Impedances)

All spectral results can be visualized graphically by pressing the right mouse button (RMB) on a selected result cell of a frequency domain result. Spectral plots resp. impedance plots are available for the following result types:

- Electric field strength
- Impedance of the power bus and DeCaps
- Noise voltage due to switching currents
- Common mode voltage due to the signal current per E-net.



## Zooming

- Within these plot windows you can always **zoom in** by opening a rectangle with the left mouse button pressed. Using the middle mouse button, the zoom area returns to the previous state.

## Scaling

- The type of scaling (linear or logarithmic) and the displayed ranges can be controlled individually for the x- and y-axis within the **Option Dialog**, depending on the content of the plot. The frequency axis will always be displayed in the same manner, hence the setting for this axis can be done within the General Tab of the Options Dialog.

## Units

- The units can be changed within the Options Dialog, General Tab or within the toolbar, if this is enabled in the Options Dialog.



# Time for a break...

