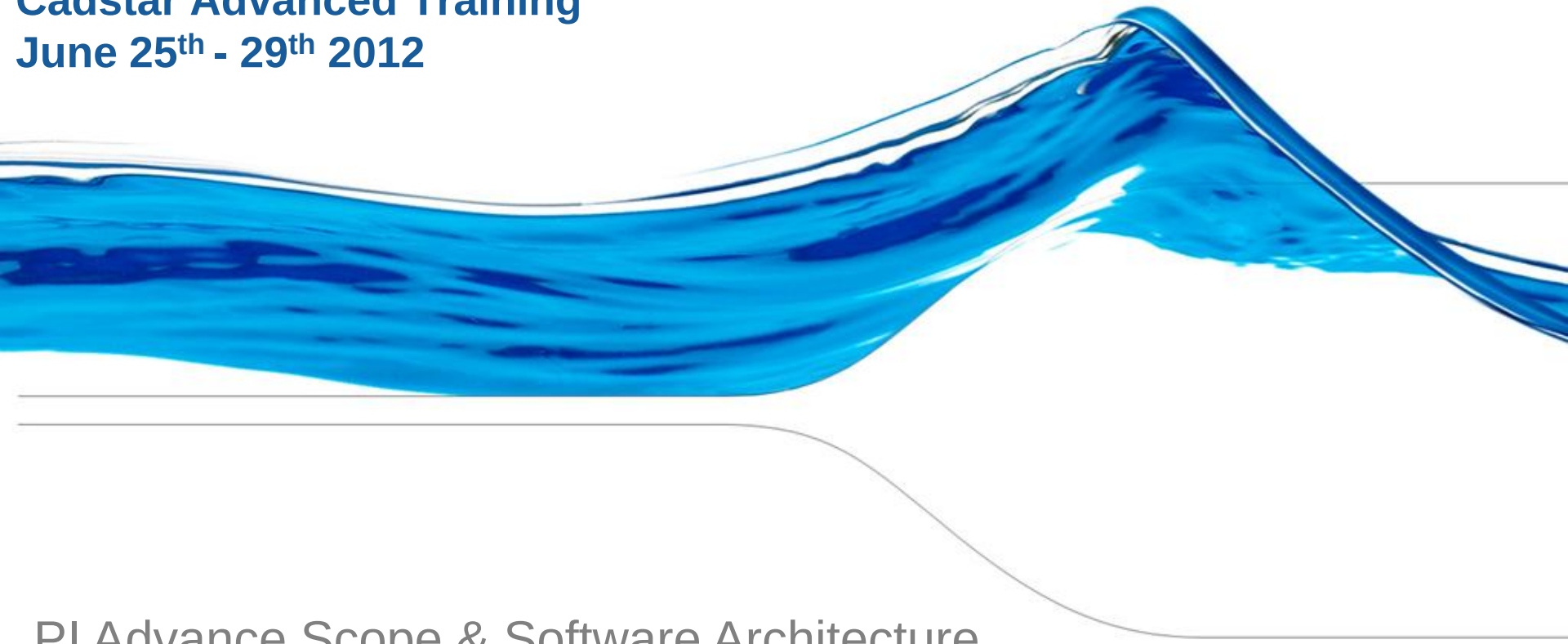
Cadstar Advanced Training
June 25th - 29th 2012



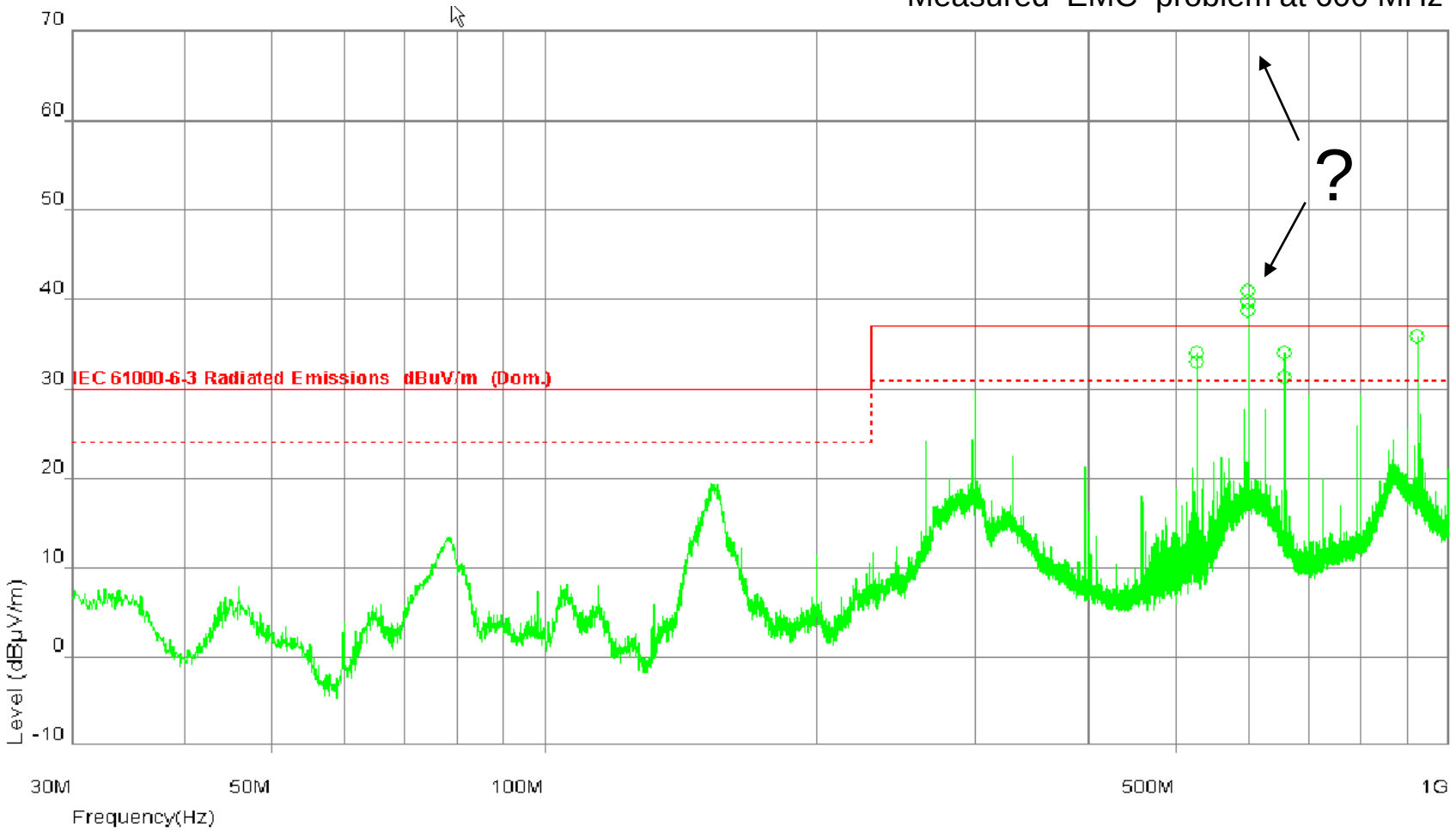
PI Advance Scope & Software Architecture

Ralf Brüning
Product Manager High Speed Design Solutions/ Senior Partner
Zuken EMC Technology Center Paderborn

EMC and PCBs ?

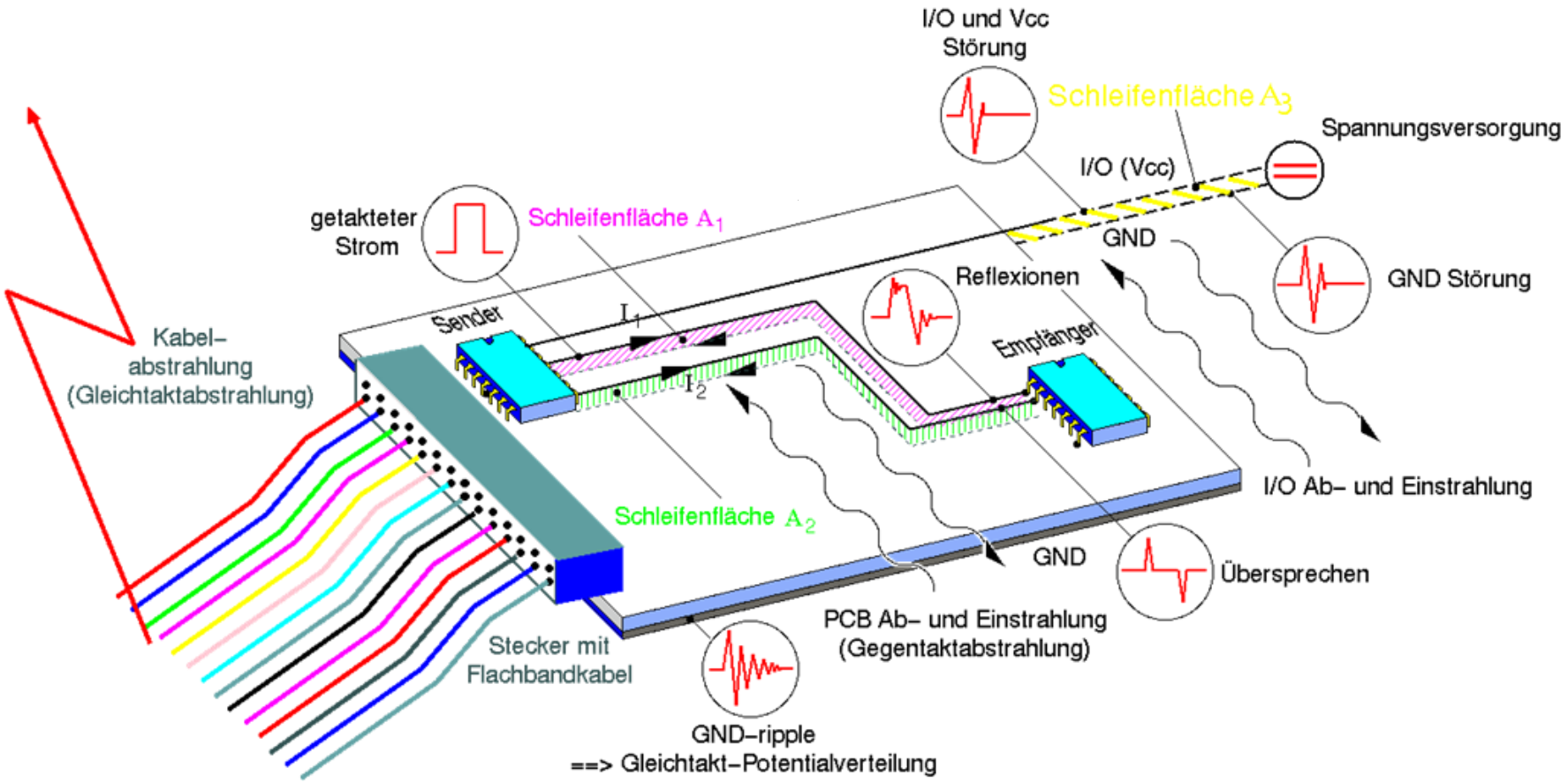
EMC measurement result:

Measured EMC problem at 600 MHz



EMC-Mechanisms on PCBs

The "EMC-Nightmare" of a PCB



Some Basics #0

Decibel ? Why dB ? What is that ?

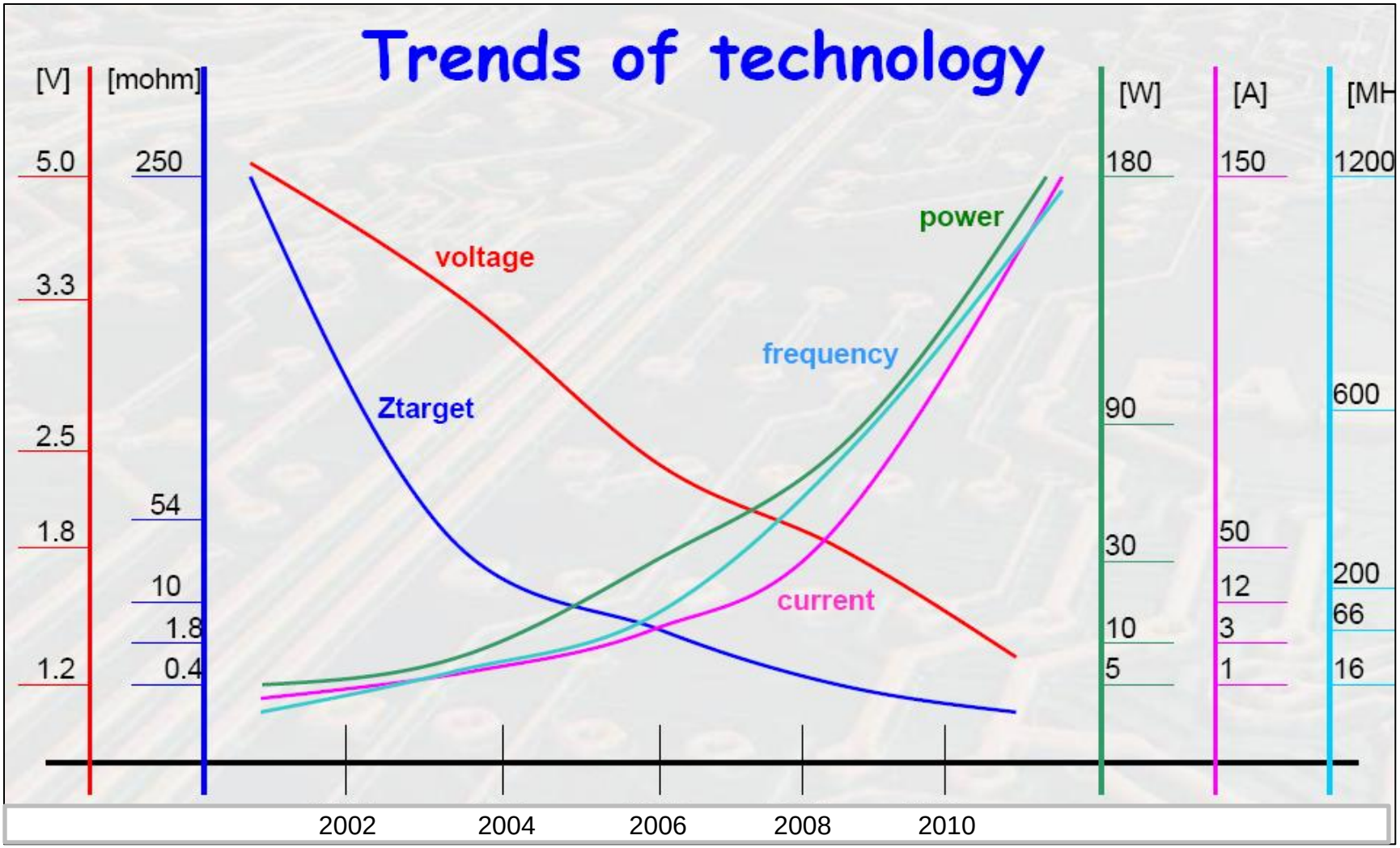
Decibel notation will characterize the relation or proportion between 2 quantities rather then giving just single value

$$r = 10 \cdot \log_{10}\left(\frac{P_1}{P_2}\right) = 10 \cdot \log_{10}\left(\frac{U_1^2/R}{U_2^2/R}\right) = 20 \cdot \log_{10}\left(\frac{U_1}{U_2}\right)$$

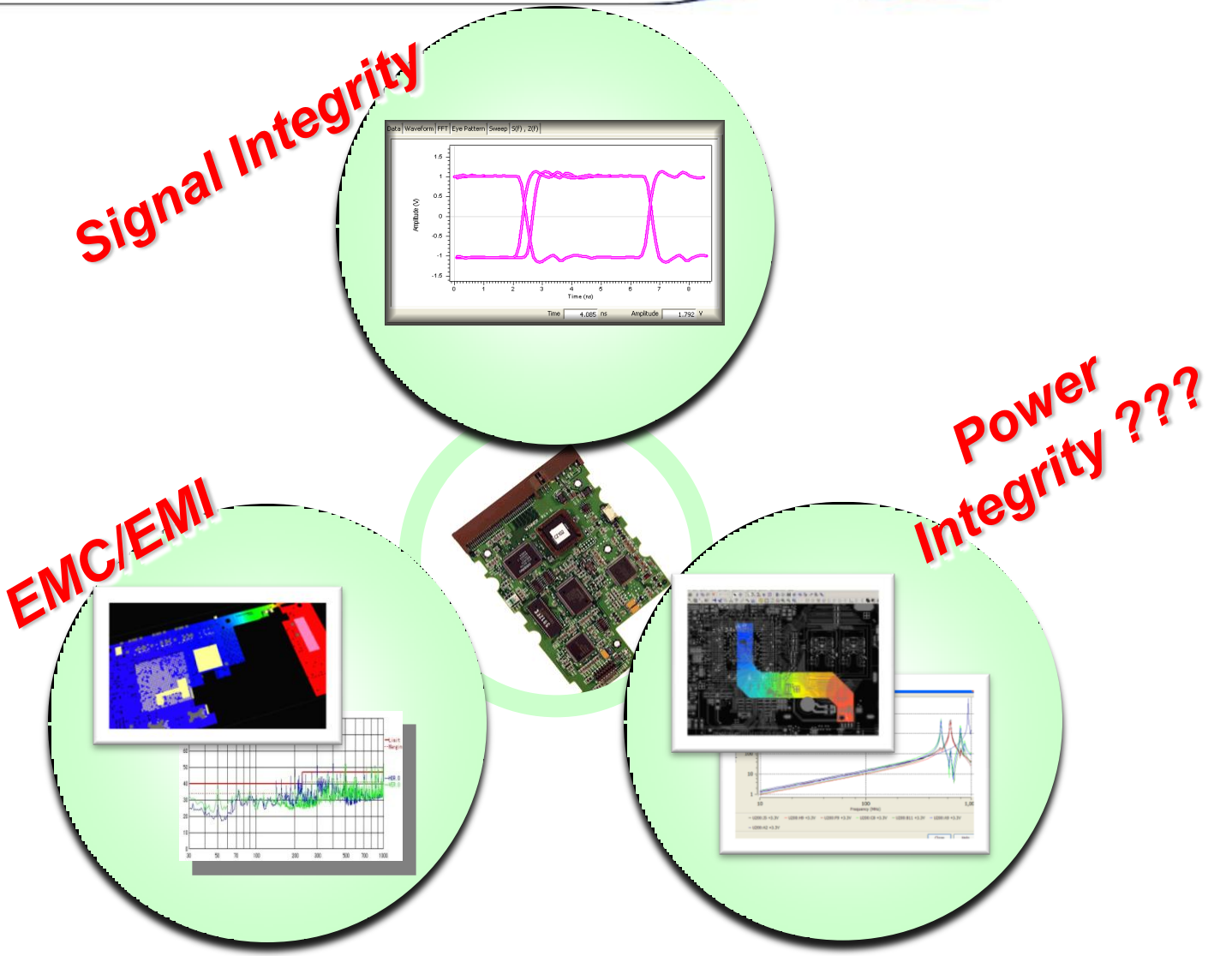
$$dB\mu V \equiv 20 \cdot \log_{10}\left(\frac{\text{U in V}}{1\mu\text{V}}\right)$$

Ratio	dB
1000000	120
100000	100
10000	80
1000	60
100	40
10	20
5	13,98
3	9,54
2	6,02
1	0
0,1	-20
0,01	-40
0,001	-60

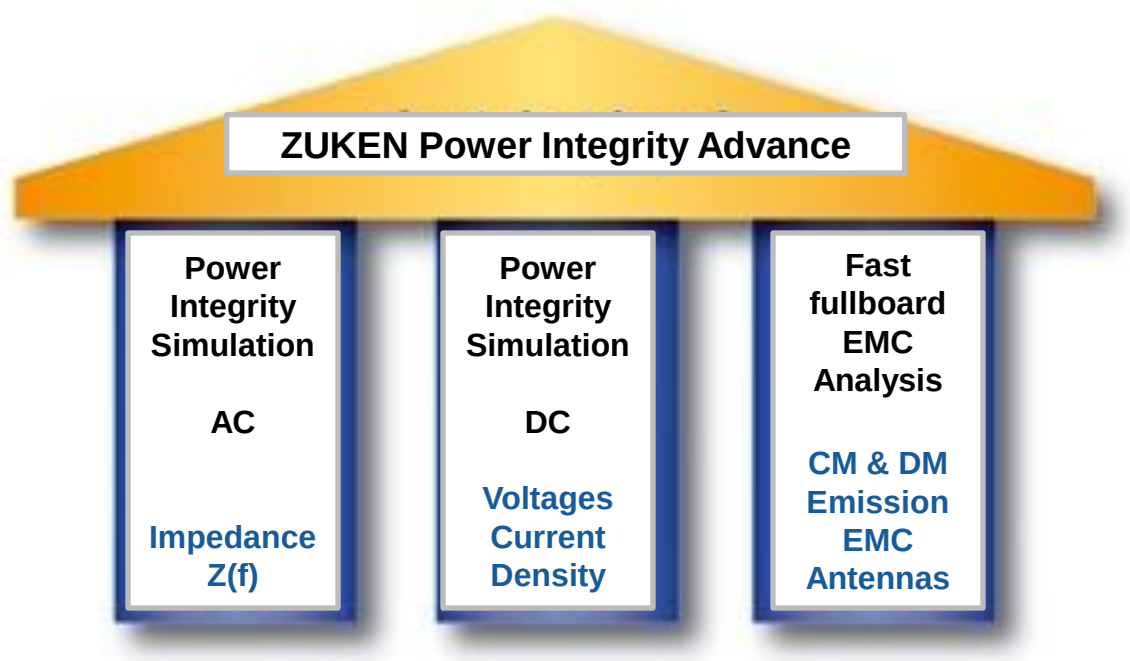
Electronic Design Trends



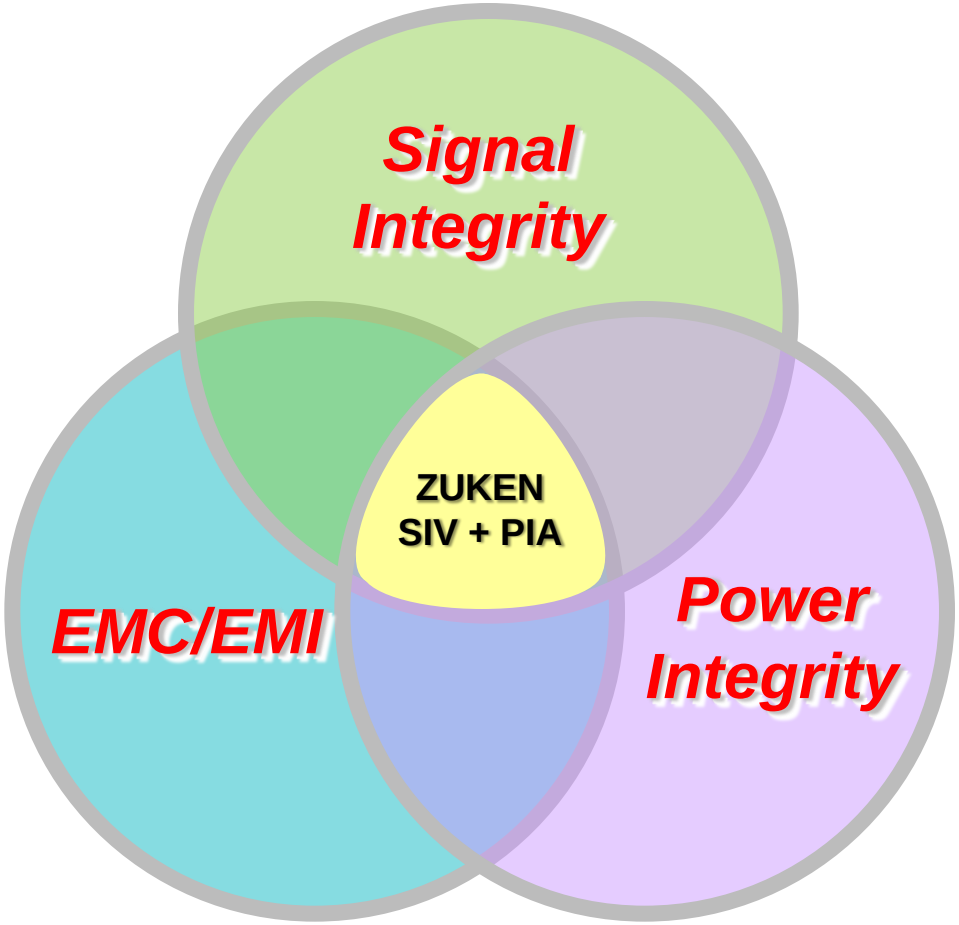
The Good Old Days: Verification Disciplines separated (or not needed at all)



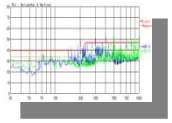
The 3 Functional Columns of Power Integrity Advance



Today: Concurrent Approach Needed

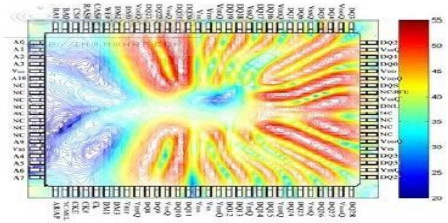


→ What causes PCBs to radiate ...



- **Overall PCB Radiation**
  - **Differential Mode (from Transmission Lines)**
  - **Common Mode Radiation**
    - **Voltage Driven**
      - **Direct**
      - **Crosstalk driven I/O nets**
    - **Current Driven**
      - **Ground Noise/ Plane Inductivity**
  - **Radiation from Power Distribution**
    - **Direct**
    - **Cables**

plus ….



The Idea behind: UMR EMC-Expert System Approach

- Modular *new* approach to EMC analysis: separated into single algorithms, covering a specific EMI effect, individually
- Based on available information about ICs, (i.e., circuit models, IBIS)
- Therefore shares/utitlizes information which might be already inhouse (SI simulation process)
- Treating:
  - ✓ **Differential-** & **common mode** radiation
  - ✓ **Power Bus** analysis
- Verified by measurements & numerical computations (at UMR and their partners)
- Goals:
  - Fast identification of critical areas & configurations
  - Estimation of potential radiation levels
  - Usable within the design-flow, by **non-experts**, too!

The EMC-Expert System Approach

The EMC Expert System Consortium

- Mission of the University of Missouri Rolla (UMR) Expert System Consortium (EMC Consortium):

> *The software looks for EMI antennas on or off the board and evaluates how hard they are being driven. It identifies any problems found with the board layout and estimates the impact of these problems on the radiated EMI from the system*

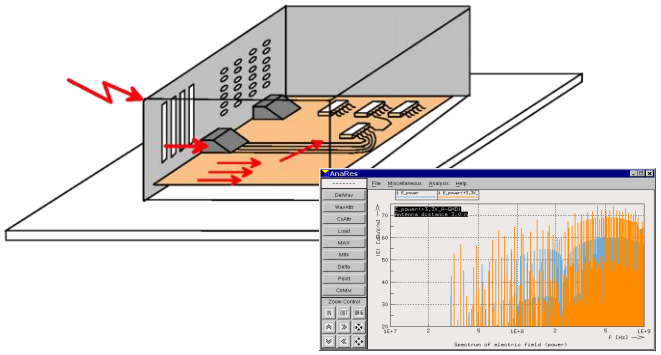
Source: www.emclab.umr.edu/consortium

- Zuken is a member of this Consortium since 1996. Other members include:

  Apple Computer Corporation, IBM Corporation, Intel, LG Corporation, Mentor Graphics, NEC Corporation, NCR, Siemens, Sony Corporation

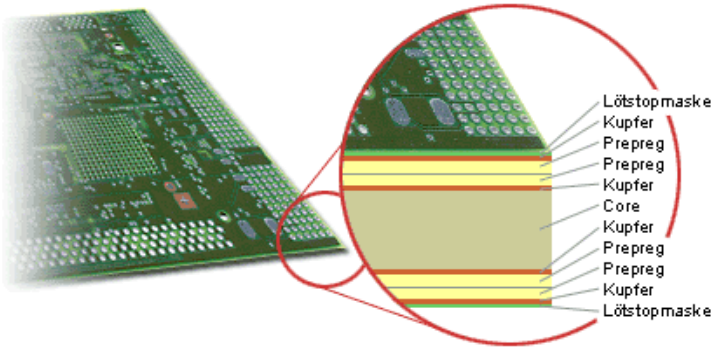
- Current research of the EMC Consortium
  - System Level EMI predictions
  - DC Power Bus analysis
  - ESD related analysis

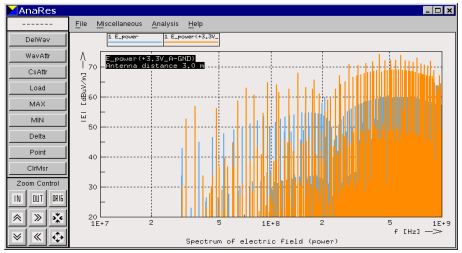
  ...



The EMC-Expert System Approach

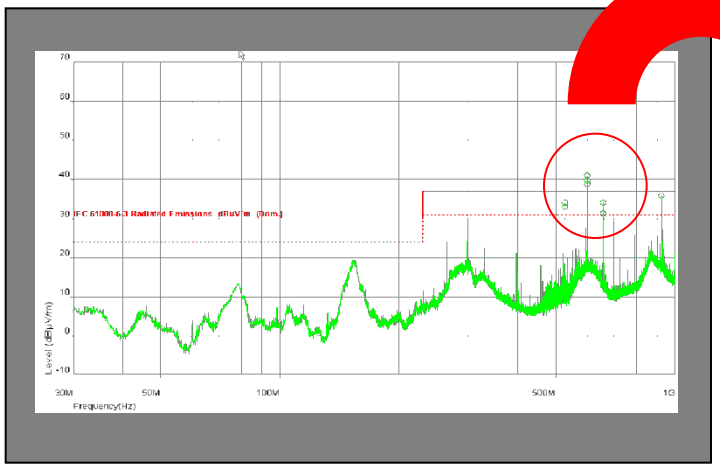
- The *EMC Expert System approach* intends to *simulate* the way how a human EMC expert will treat/solve EMC problems.
- Its not intended to compete against measurement and/or 3D solvers (as human experts won't do either)
- Its not solving Maxwell (as human experts don't do either – most of them).
- Its all about:
  - Looking the whole board at once
  - Identify and qualify potential antennas
  - Know/propose how to get rid of them
  - Predict the effectiveness of a measure with respect to EMC/far field

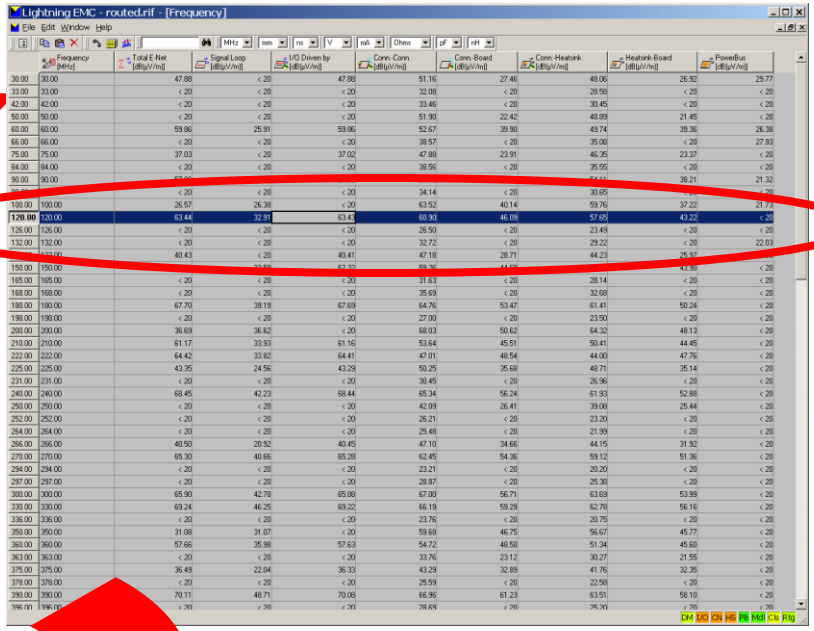




PIA EMC&PI:
Noise/Problem Source Identification

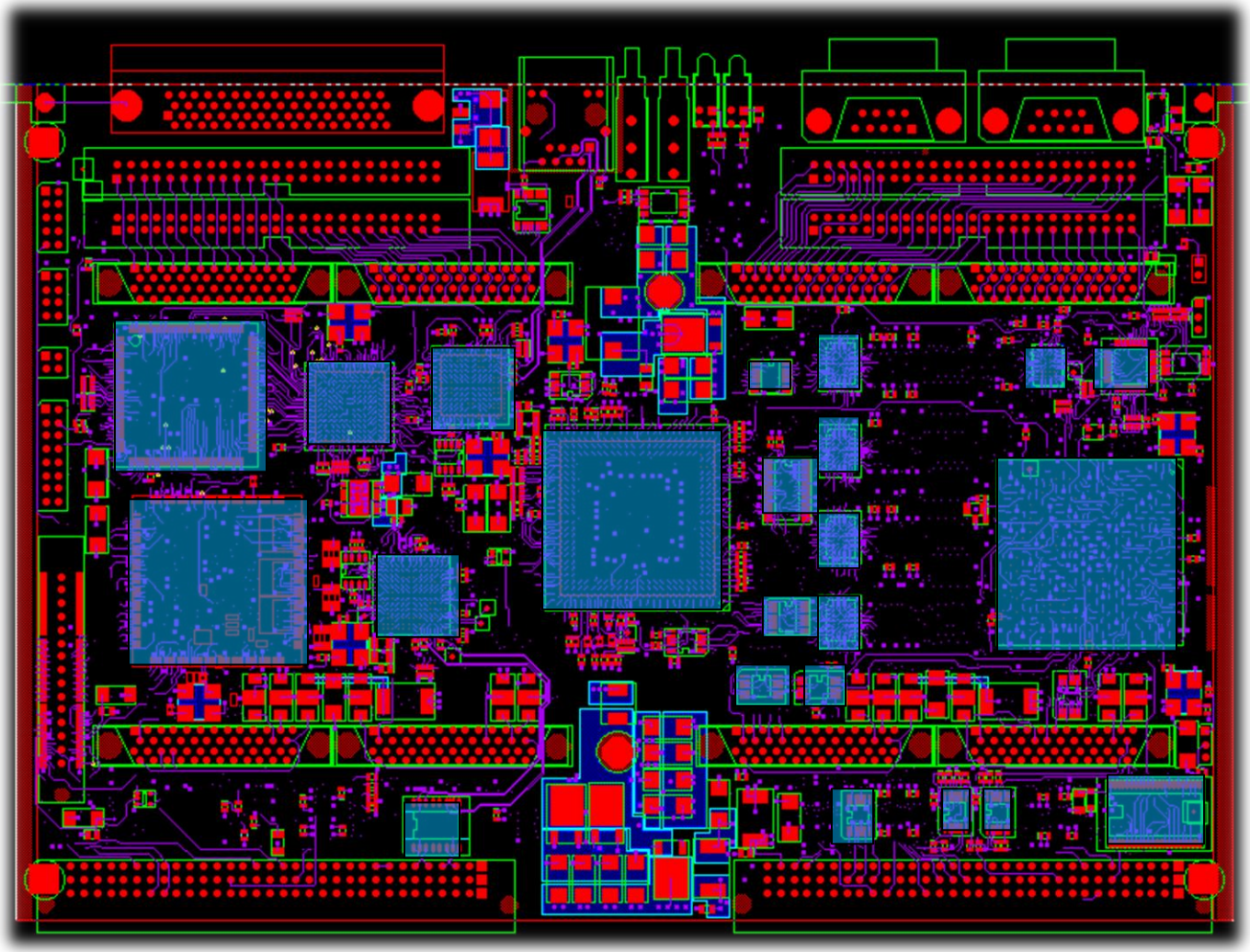
Goal: Identification of sources, contributing effects and configurations to a specific peak in the spectrum, feedback to CAD layout





A typical PCB ….
(from 2009, industry automation, Power-PC & DDR Memory)

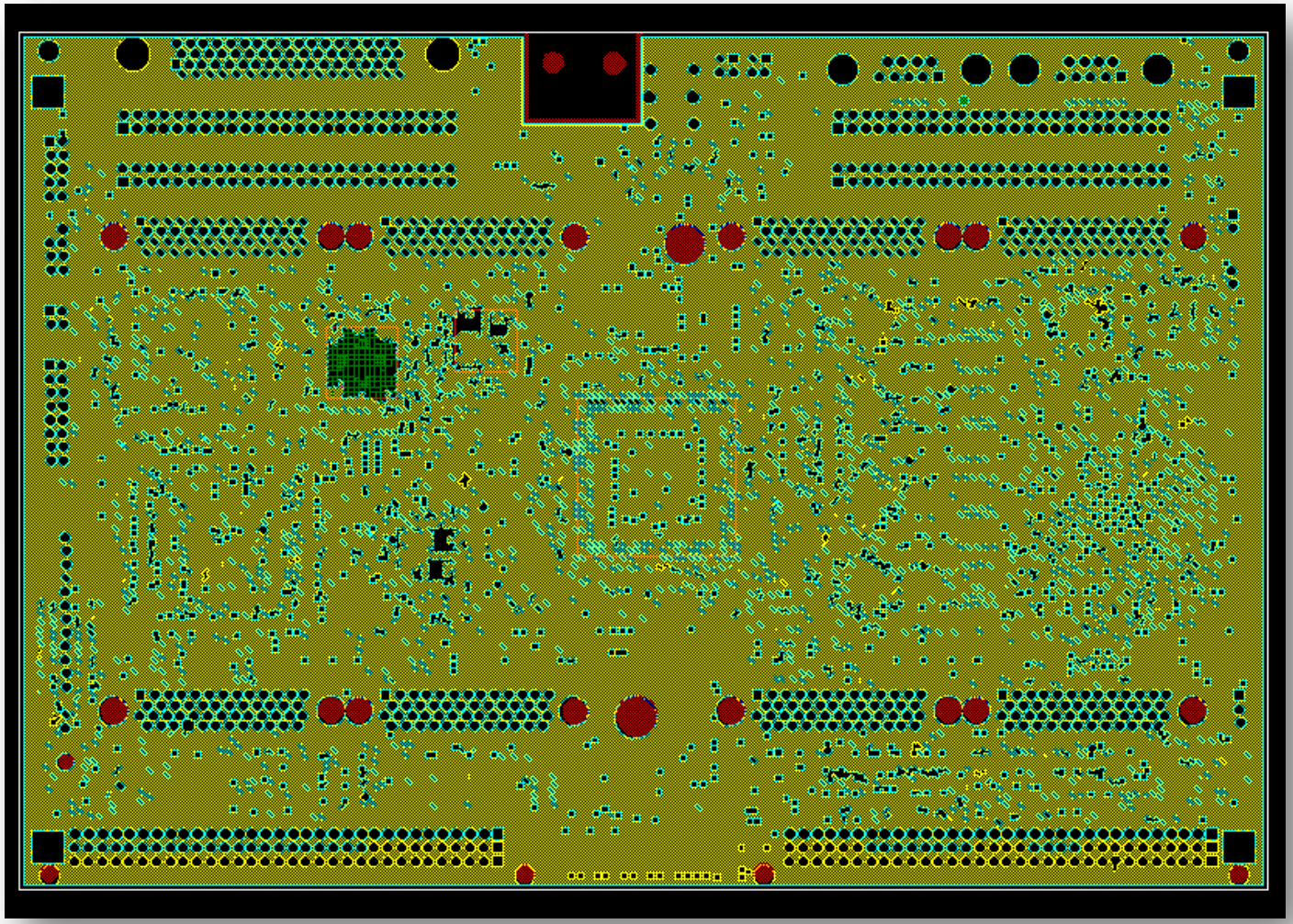
- The active devices (ICs) will consume the majority of the energy
- They need the various voltage levels to work (on this board 17 different supply and ground nets)
- Several BGAs are used on this design



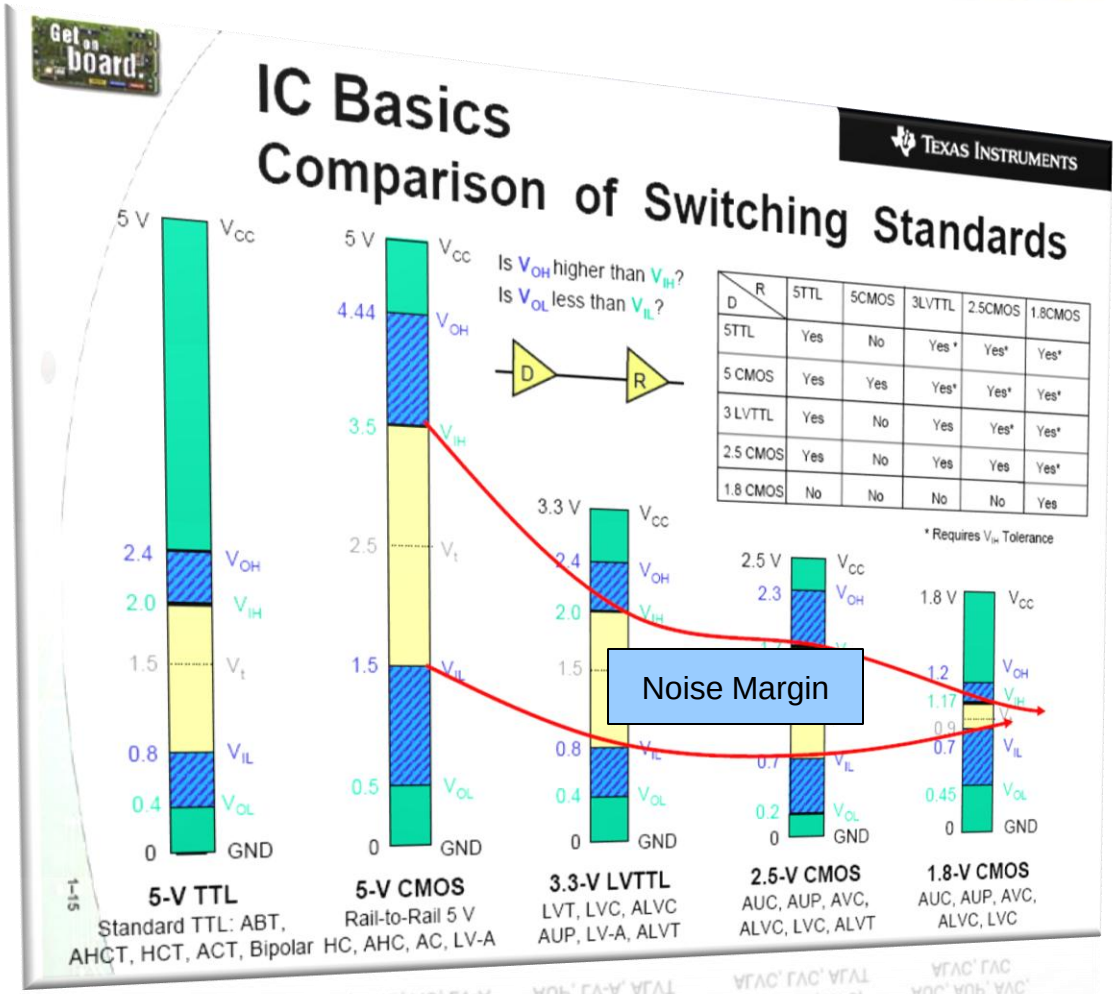
So most of our digital PCBs have things like this …. (hopefully)

What is this ???

A power distribution system (PDS)



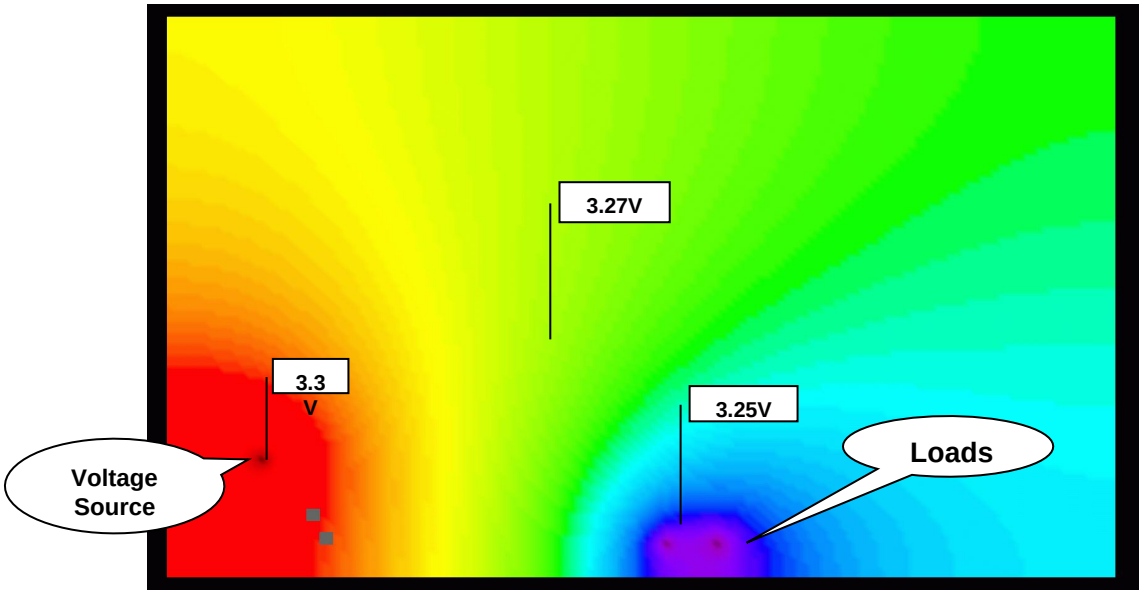
Lowered Noise Margins of todays ICs



D \ R	5TTL	5CMOS	3LVTTL	2.5CMOS	1.8CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes

Power Distribution Systems

Voltages are not equally distributed and not considered ideal over copper planes

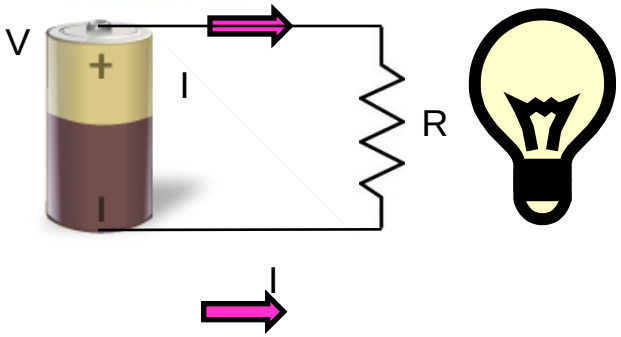


Example: 3.3V Power Distribution System

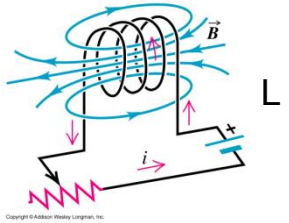
"Voltage drops" occur on the copper area and within the vias – but why ?

Basic Electrical Concepts #1

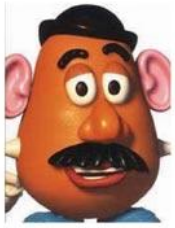
- Voltage: **Electrical potential difference** (denoted ΔV and measured in volts) between two points. A voltage may represent either a source of energy (electromotive force) or it may represent lost or stored energy (potential drop). Voltage can be caused by static electric fields, by electric current through a magnetic field, by time-varying magnetic fields, or a combination of all three.



- Current: **Electric current** is a flow of electric charge through a medium. This charge is typically carried by moving electrons in a conductor such as wire. An electric current (Amperes law) produces a magnetic field.
- No voltage without current, no current without voltage

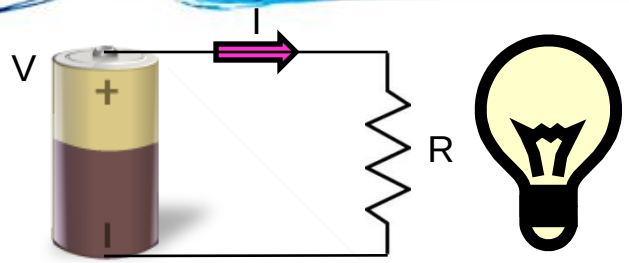


- **Ground:** Not an acceptable technical term at all (current return path is what should be used, Dr. Archembault from IBM invented the phrase that ground is a ***place to plant potatos or carrots***), so there even as well does not exist a “Ground-Bouncing” like people assume it to happen, it’s a narrowing of the potential difference

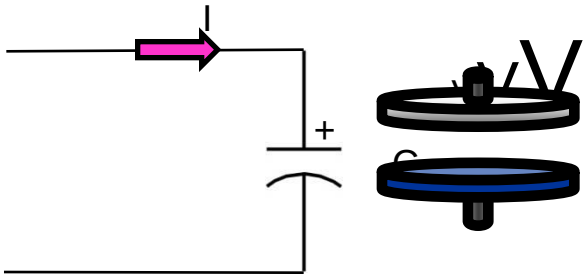


Basic Electrical Concepts #2

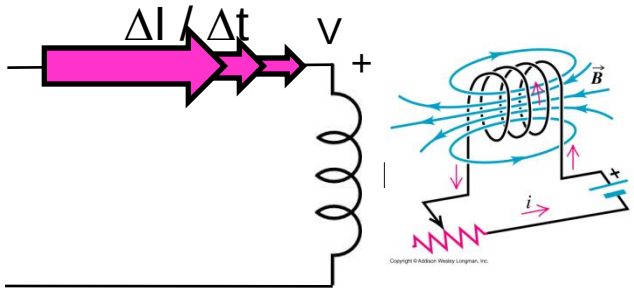
- Resistors dissipate **energy**
  - Resistance = Voltage / Current (R = V / I)
  - Voltage = Current ∗ Resistance (V = I ∗ R)



- Capacitors store **energy** in an electric field
  - Charge = Capacitance ∗ Voltage (q = CV)
  - Current (Δq / Δtime) = C ∗ (ΔV / Δt) (I = C ∗ ΔV / Δt)
  - Power plane over ground plane is a great capacitor!



- Inductors store **energy** in a magnetic field
  - Voltage = Inductance ∗ (ΔI / Δt) (V = L ∗ ΔI / Δt)
  - Oppose current changes with a voltage
  - Inductive kick: pull the plug on a vacuum cleaner when it's running!



Basic Electrical Concepts #3

- For Signal Integrity you should care for resistances and capacitances
- For Power Integrity, ***Mr. Inductance*** is the guy to care for
- Requirements do increase (i.e. JEDEC DDRx)

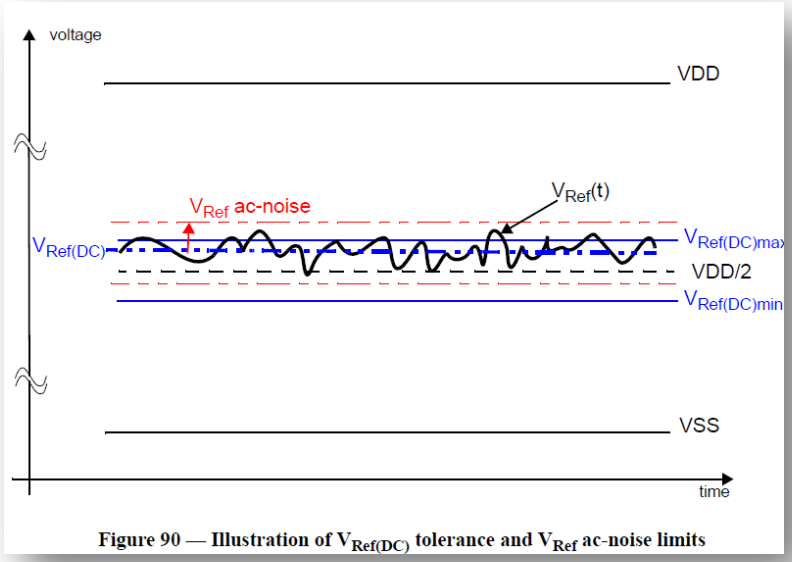
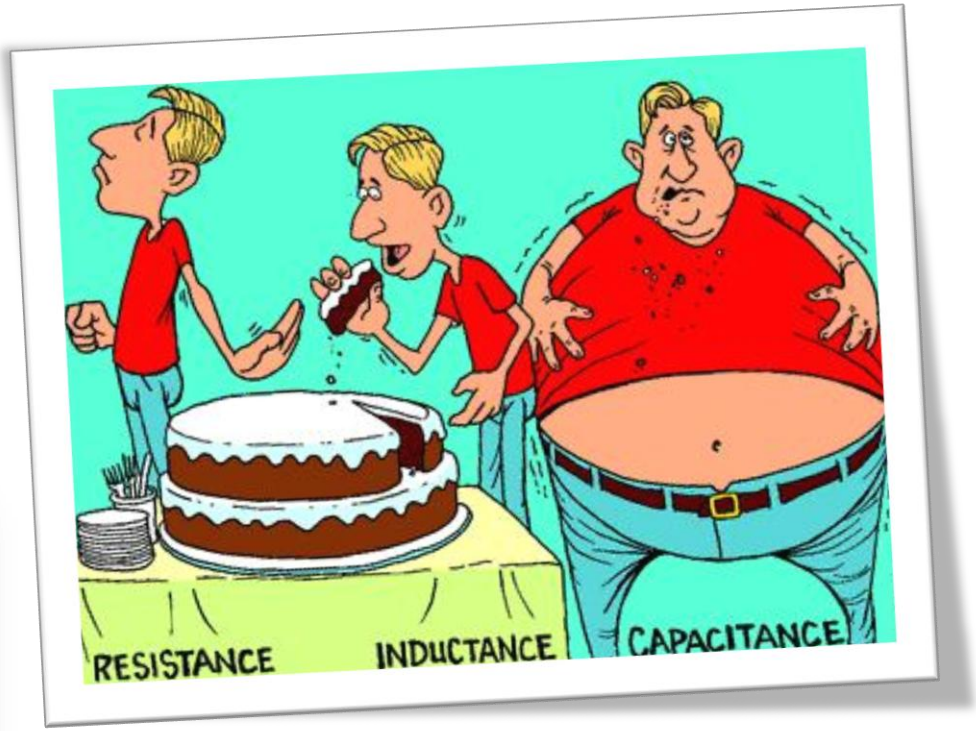
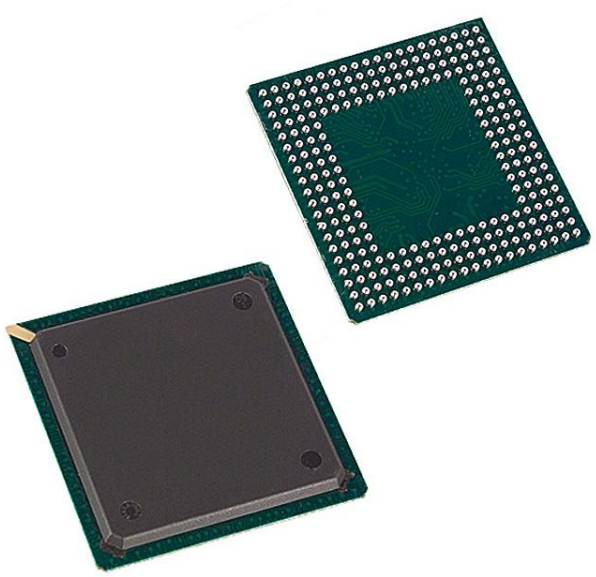


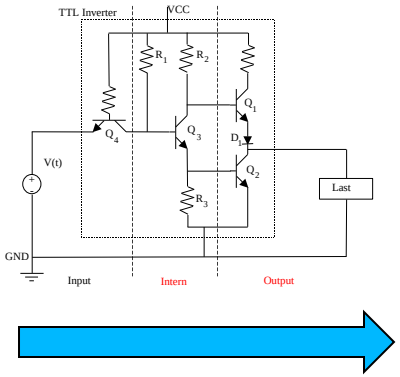
Figure 90 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits



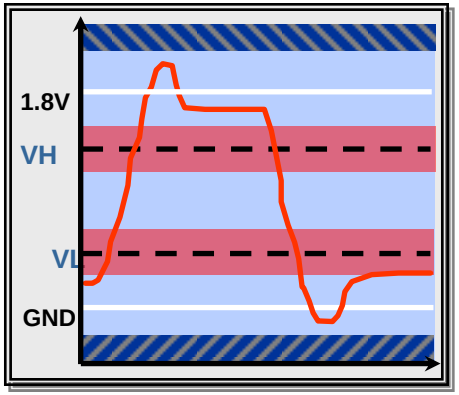
Picture © Agilent

When Integrated Circuits Switch ….



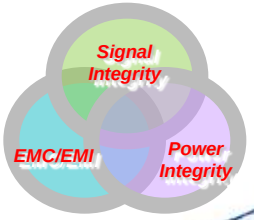


- They (should) change logic state.
- They need **charge.**
- **Voltage** has to be delivered (for reaching logic levels).
- A switching **current** will occur !

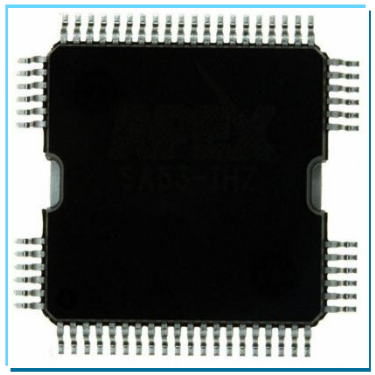


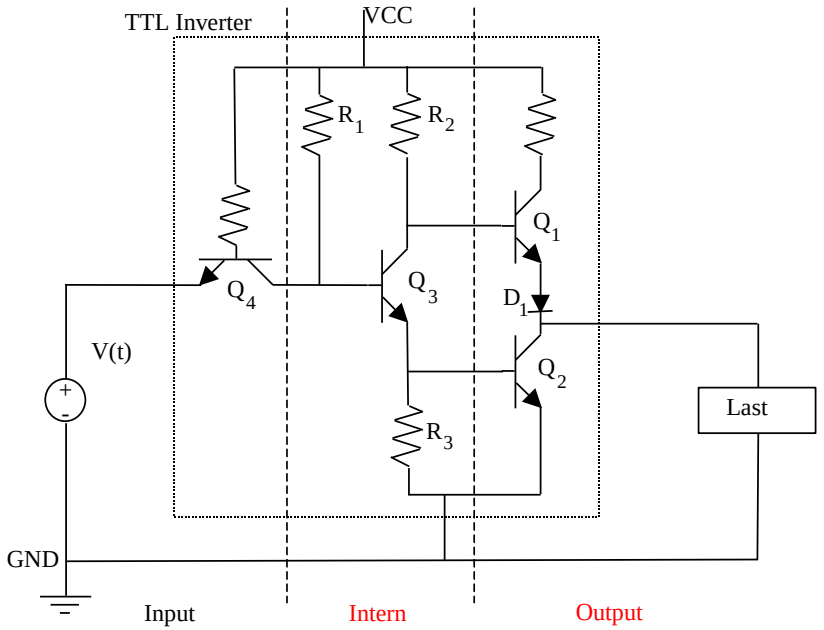
Relation between voltage & current ? → **Ohm's law**

Power Integrity: Switching Current



- IC Switching *current* depends on:
  - Number of active outputs
  - Activity state
  - Driver rise and fall times
  - Clock frequencies
  - Load conditions





Do you have to worry ?

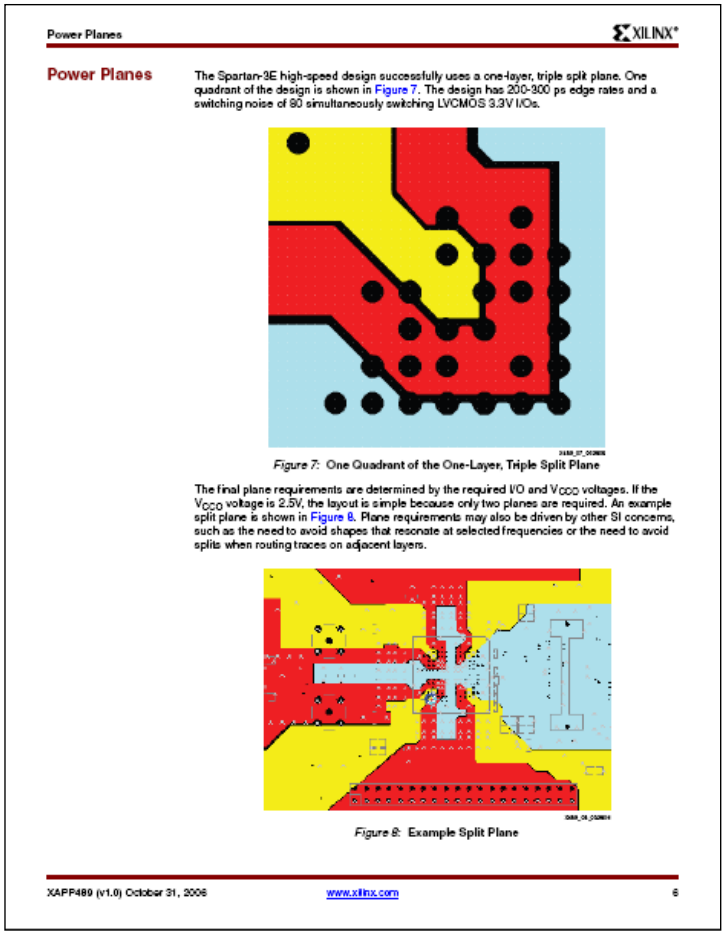
It depends … but I think YES !

Design *Challenges* increase dramatically !

(Example: Xilinx design guides for Xilinx Spartan FPGAs)

PDS Design for FPGAs

- One capacitor per Vcc pin
- Yes, EVERY Vcc pin – Vccint, Vcco, Vccaux, Vref
- Within the total count for each supply:
  - Allocate some in each frequency range
    - 3% 680 uF
    - 7% 2.2 uF
    - 15% 0.22 uF
    - 25% 0.047 uF
    - 50% 0.001 uF
- Power planes and/or sandwiches are a must



Power Planes

Power Planes

The Spartan-3E high-speed design successfully uses a one-layer, triple split plane. One quadrant of the design is shown in Figure 7. The design has 200-300 ps edge rates and a switching noise of 80 simultaneously switching LVCMOS 3.3V I/Os.

Figure 7: One Quadrant of the One-Layer, Triple Split Plane

The final plane requirements are determined by the required I/O and V_{CCO} voltages. If the V_{CCO} voltage is 2.5V, the layout is simple because only two planes are required. An example split plane is shown in Figure 8. Plane requirements may also be driven by other SI concerns, such as the need to avoid shapes that resonate at selected frequencies or the need to avoid splits when routing traces on adjacent layers.

Figure 8: Example Split Plane

XAPP489 (v1.0) October 31, 2006 www.xilinx.com 6

Pictures © Xilinx

Evolution of Power Distribution Systems

- The requirements on power distribution systems have changed in the last 20 years.
- CMOS voltages are decreasing while more pins can switch simultaneously, inducing serious switching current (and more power consumption), at higher frequencies.
- Matching the *target impedance* (ratio of voltage/current while switching) the power distribution system is a key problem in modern high speed designs.

Year	Voltage (V)	Current (A)	Max-Pins (IC)	Z_{target} (mΩ)	f [MHz]
1990	5	1	68	250	16
1994	3.3	3	244	50	66
1998	2.5	12	>500	10	233
2002	1.8	50	>1200	2	800
2006	1.5	> 100	> 2000	0.5 - 1	> 2GHz
2010	1.0	Several hundred	> 4000	<< 1	> 3 GHz

Basic Electrical Concepts #4

- We do have the relation between voltages (to be supplied) and currents (occurring) → Ohms law describes that can be applied for the relation between voltage, current and impedance
- Resistance in the PCB design world goes to become impedance (ratio between voltage and current in the switching process)
- Please Note: This is a different impedance the characteristic impedance of signal traces (means, computed differently)
- Silicon vendors nowadays define Ztarget as requeriment/constraint

Table 1. PowerPC Processor Parameters

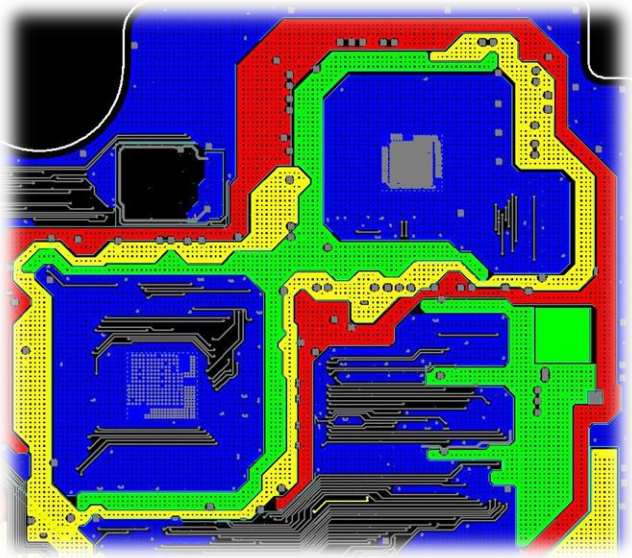
Processor	Parameter							No. of V_{DD} pins	Notes
	V_{SUPPLY}	P_{MAX}	I_{MAX}	V_{RIPPLE}	$V_{RIPPLEPCT}$	di/dt	Z_{TARGET}		
MPC8245 @ 300 MHz	1.8 V	2.2 W	1.22 A	± 100 mV	5.6%	0.1 A/ns	83 mΩ	20	1,2
MPC8245 @ 466 MHz	2.1 V	3.1 W	1.47 A	± 100 mV	4.8%	0.1 A/ns	69 mΩ	20	1
MPC7410 @ 500 MHz	1.8 V	11.9 W	6.61 A	± 100 mV	5.6%	0.2 A/ns	15 mΩ	18	1
MPC7445 @ 867 MHz	1.3 V	21.0 W	16.15 A	± 50 mV	3.9%	0.2 A/ns	3.1 mΩ	21	1
MPC7457 @ 1267 MHz	1.3 V	25.6 W	19.69 A	± 50 mV	3.9%	0.2 A/ns	2.6 mΩ	21	1,3
MPC7447A @ 1420 MHz	1.3 V	30.0 W	23.08 A	± 50 mV	3.9%	0.2 A/ns	2.2 mΩ	21	1

- The allowed voltage tolerance (voltage ripple) must be known/defined (usually around 5 %) to derive Z_{target}

$$Z_{Tagret} = \frac{(Power\_Supply\_Voltage) x (Ripple\_Tolerance)}{Dynamic\_Current}$$

Voltage Supply for ICs: Power Distribution System (PDS)

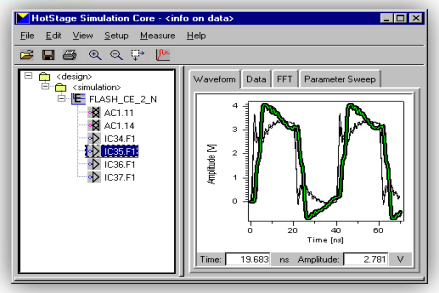
- The power distribution system (PDS) will provide voltages and deliver ***charge*** to the ICs on a PCB
- Charge on the board must be supplied over a broad frequency range:
  - Low frequency activities (we still have them)
  - In MHz range for CPU-peripheral interfaces
  - At the clock frequency (several hundreds of MHz)
  - **Provide a low impedance path for parasitic voltages at various harmonics of the clock**



Power Integrity Objective

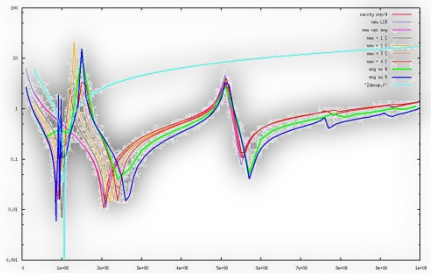
Power Integrity ?

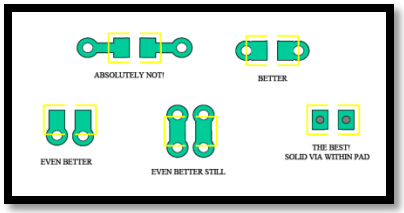
Power Integrity ⇔ Ensure proper behaviour of power distribution systems (PDS) (ako *Integrity* behaviour of power supply system)



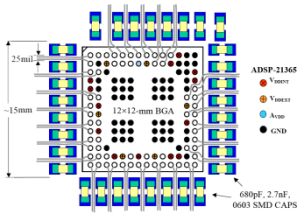
PCB Design today → Increasing challenges, complexity is growing continiously:

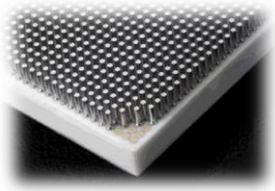
- Faster data rates (i.e. serial interconnects)
- Super-complex devices (several 1000 pins)
- Very fast memory interfaces (DDR2 interfaces common, i.e. on ASIC cells and/or FPGAs)
- Increased number of power supplies (dozends)
- Increased power consumption, problems with large currents and thermal management
- Requirements beyond *classical* SI constraints (i.e. target impedances and decoupling requirements for CPUs or FPGAs)



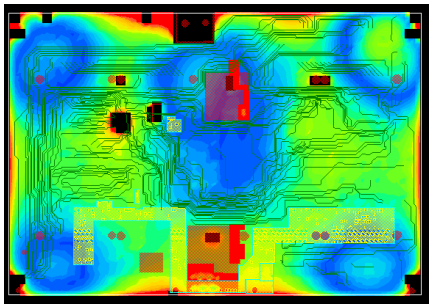


Pictures © AMD and IBM

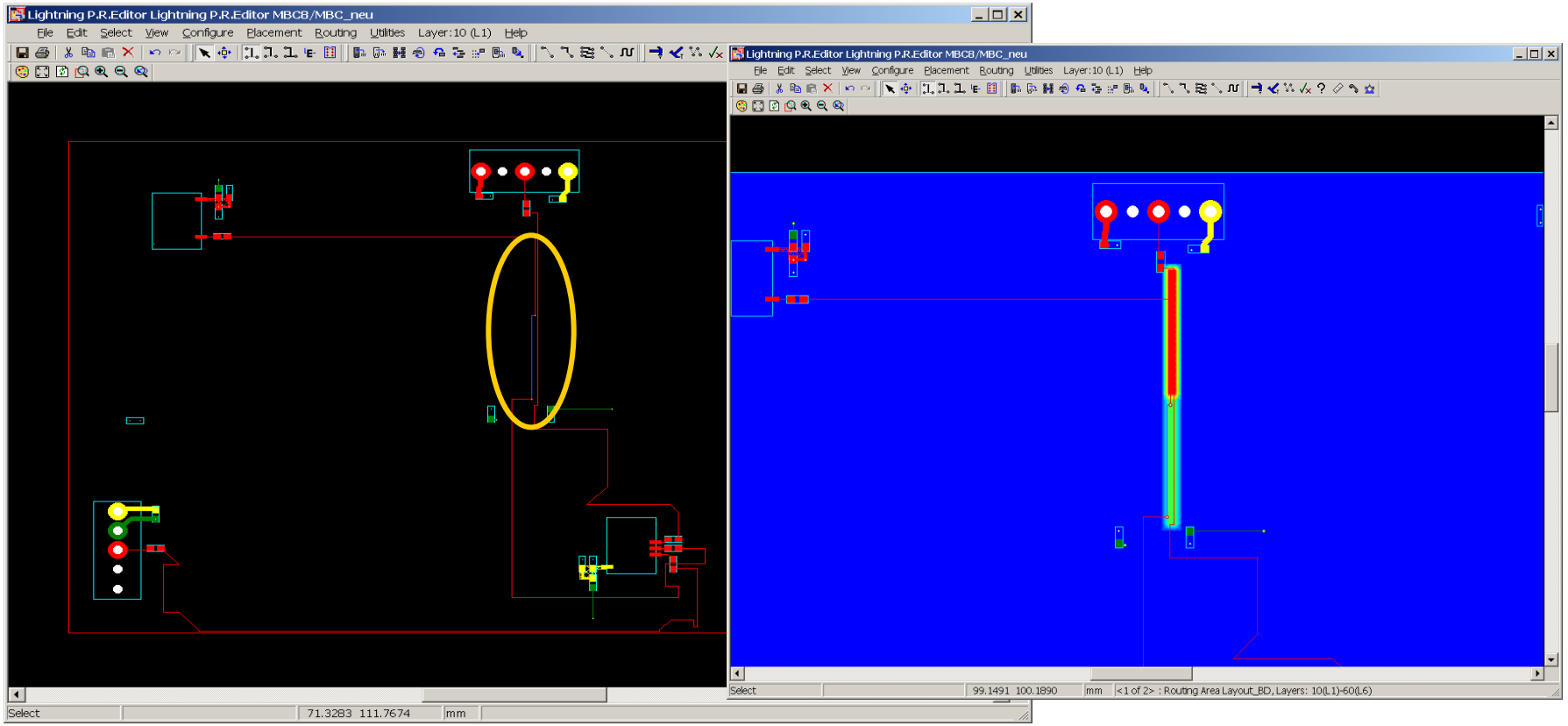


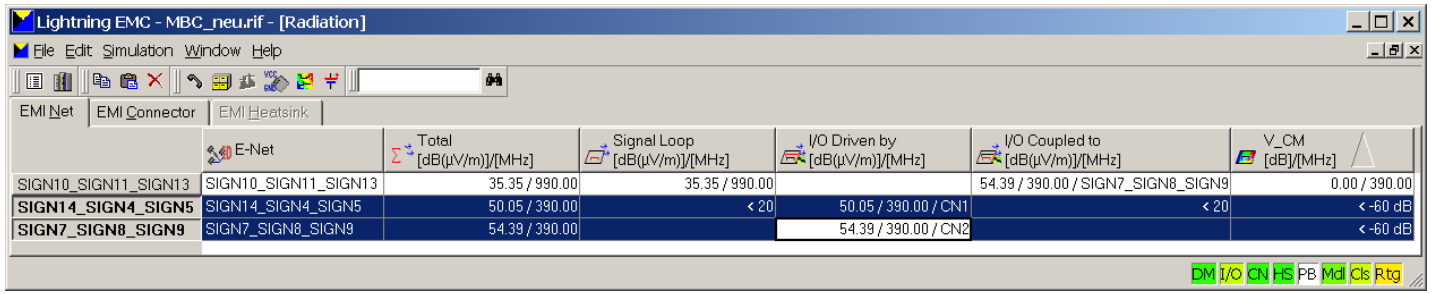


2577 pin CCGA

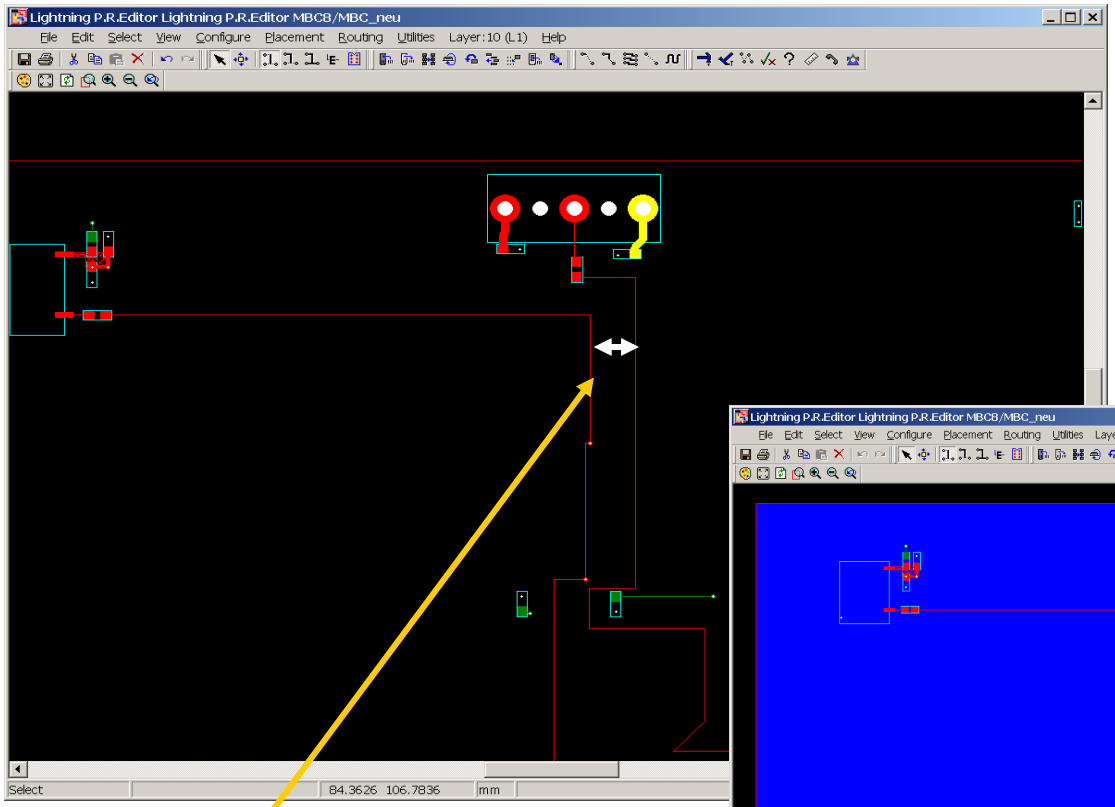


EMC-What-Ifs: Show Field Hot-Spots & Coupling Voltages, fix problems on the fly

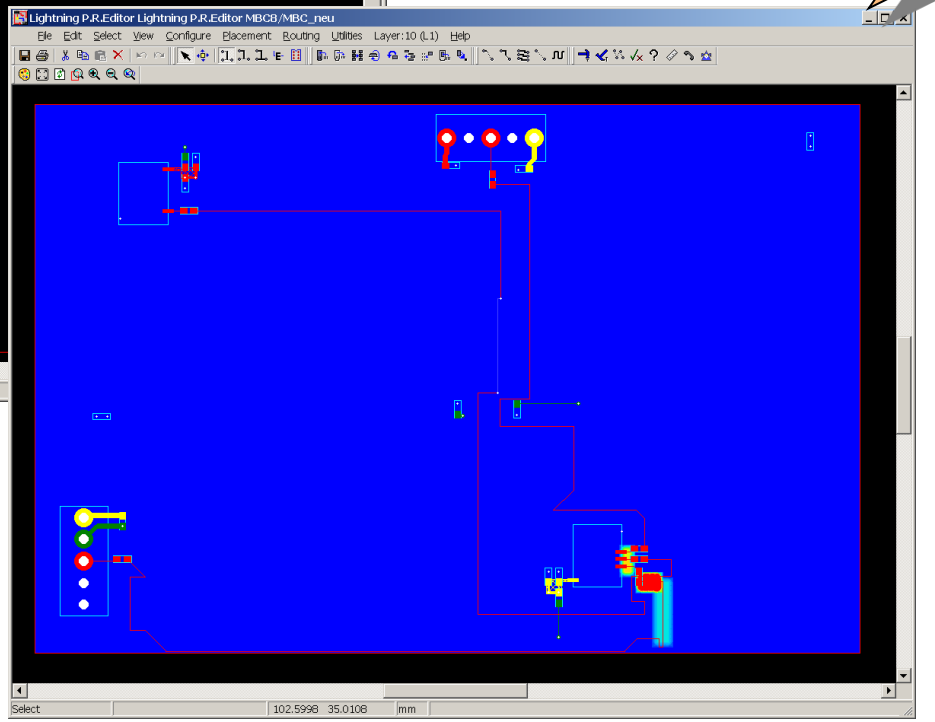




EMC-What-Ifs: Show Field Hot-Spots & Coupling Voltages, fix problems on the fly



Increase spacing



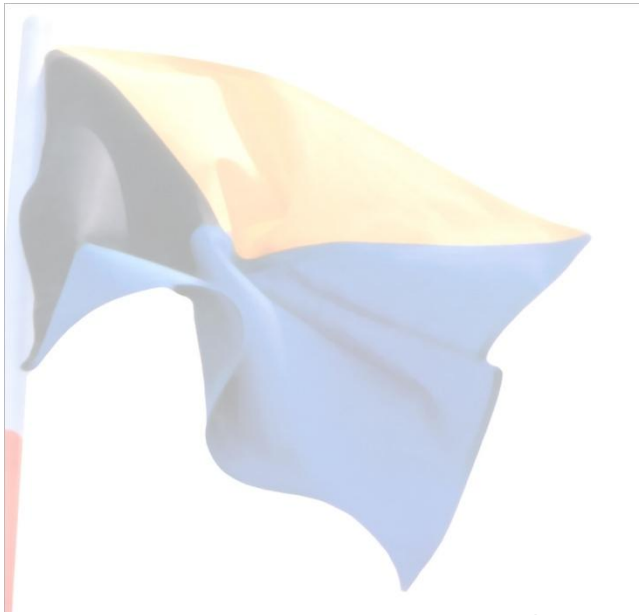
Benefit

Allow quick EMC-What-Ifs with respect to EMC noise caused by coupling structures.

Questions before the coffee break ….

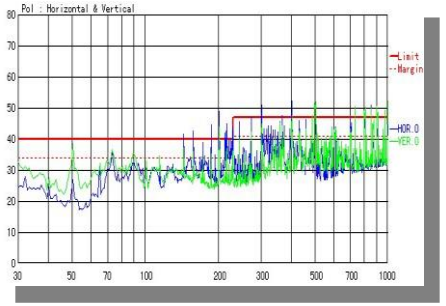
What are the 4 key features of PIA EMC Analysis ?

1. It screens complete boards !
2. Its FAST (to be used in design process)
3. It identifies EMI sources (root causes) in form of structures on PCB (nets, ICs, connectors etc.)
4. It allows EMC and PI what-ifs



Typical Ways of Treating EMC:
Design Guidelines, Measurement (& Consultancy)

Typically during PCB design EMC issues are covered upfront by design guidelines and then in prototype stage by doing measurements.



If this won't succeed, often external or internal EMC experts are asked for help.

But EMC Design rules will not make a good circuit board designer and measurement will not detect concrete error sources.

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

Maxwell Equations ?

And, experts are limited/rare (and not cheap).

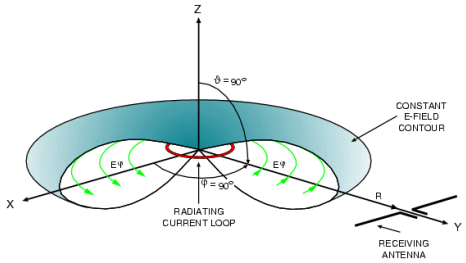
<u>So designers should:</u>

1. Use common sense !
2. Visualize and analyze signal current paths
3. Locate parasitic antennas and crosstalk paths
4. Be aware of potential EMI sources and antennas
5. Use software tools which will help/automate steps 1.-4.
   → Lightning PIA EMC approach

EMC Mechanism: Differential Mode Radiation

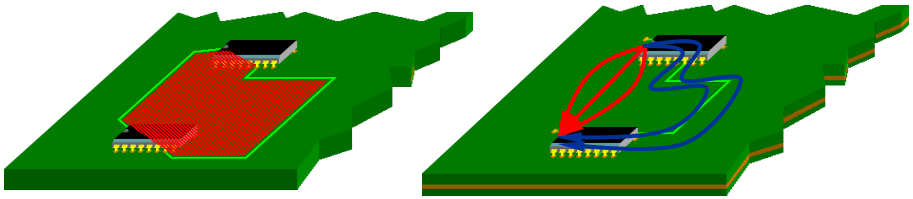
Radiated emissions due to current loops created by signal traces and return paths

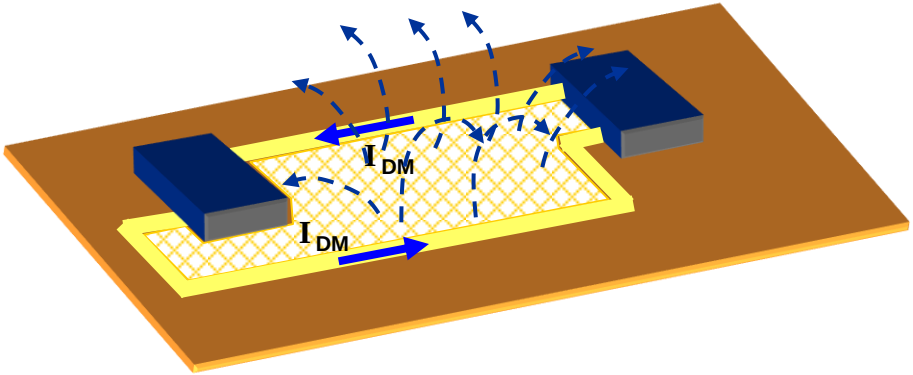
- Large current loops created by signal and GND *traces*
- GND planes decrease loop areas drastically



Main parameters are:

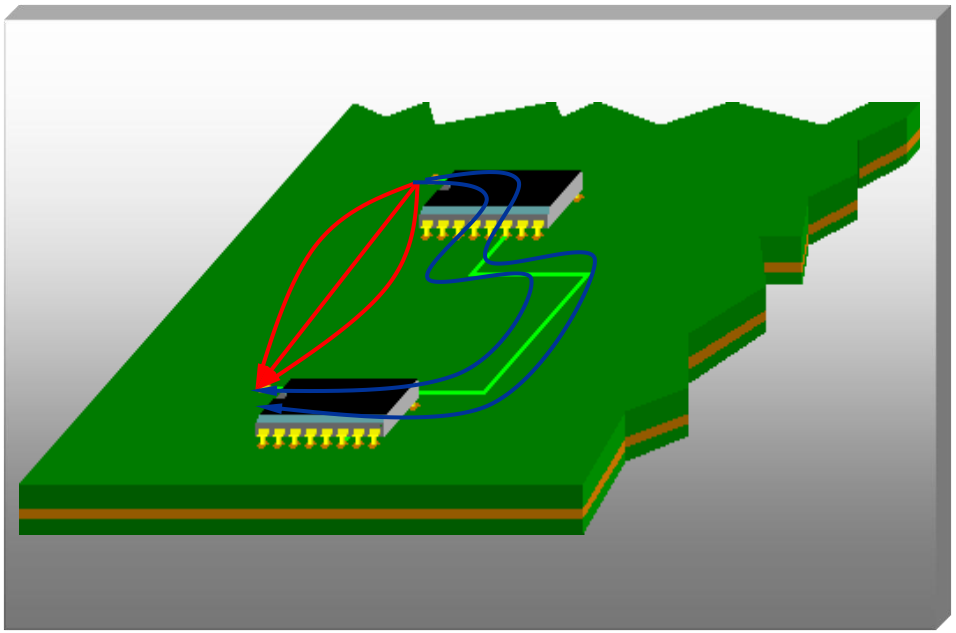
- Spectrum of the signal current I(f) (Driver, Receivers, Terminations, etc.)
- Frequency f
- Loop Area A (distance to next reference plane of each net-segment)
- Distance to closest trace (trace length on top or bottom layer)

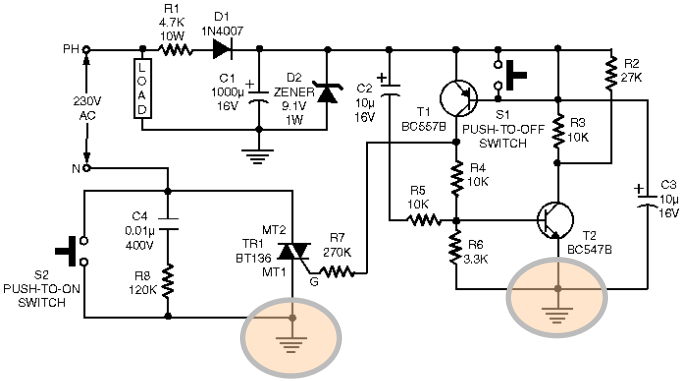




Return Currents

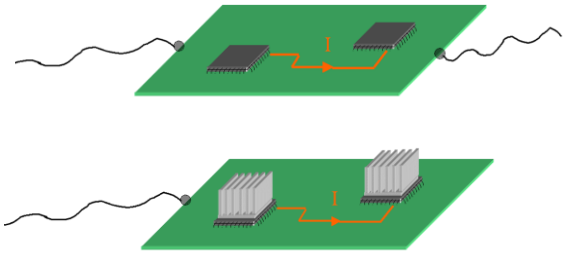
- Currents <u>always</u> returns to their source!
- They usually take the path:
  - of least impedance (for frequencies > 1MHz)
  - Not the path of the least resistance, only at very low frequencies, around 10 kHz)
  - of course not the path of shortest distance or most convenient/nicest routing path
- Current loops create inductance !
- “Ground” is not an acceptable technical term.

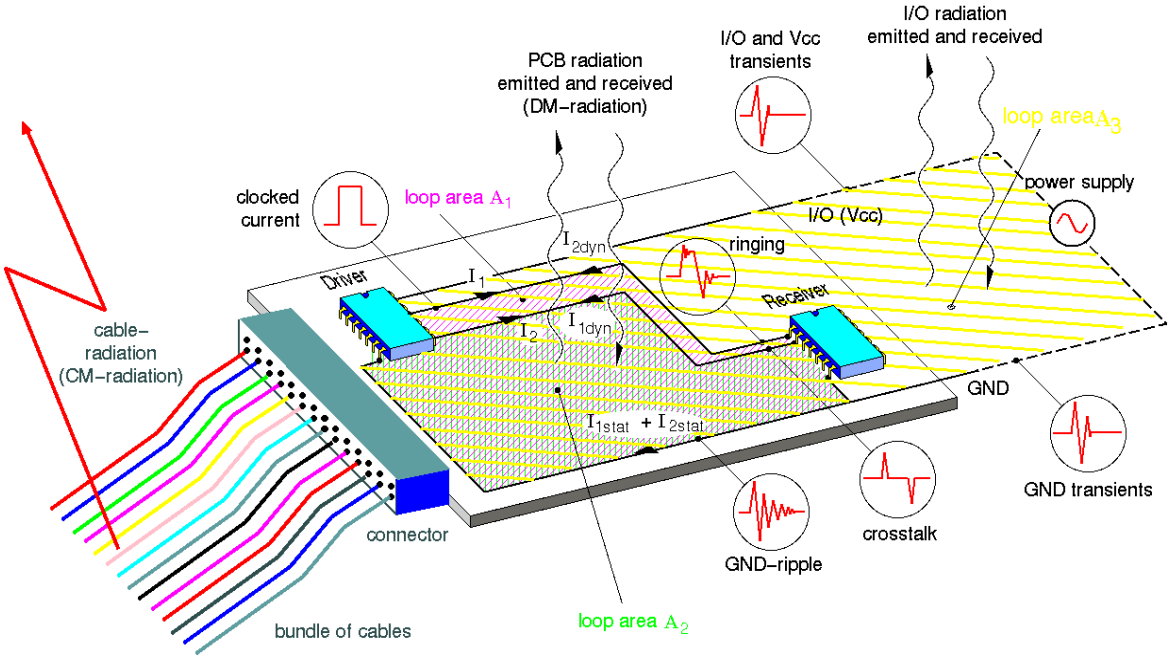




EMC Mechanism: Common Mode Radiation

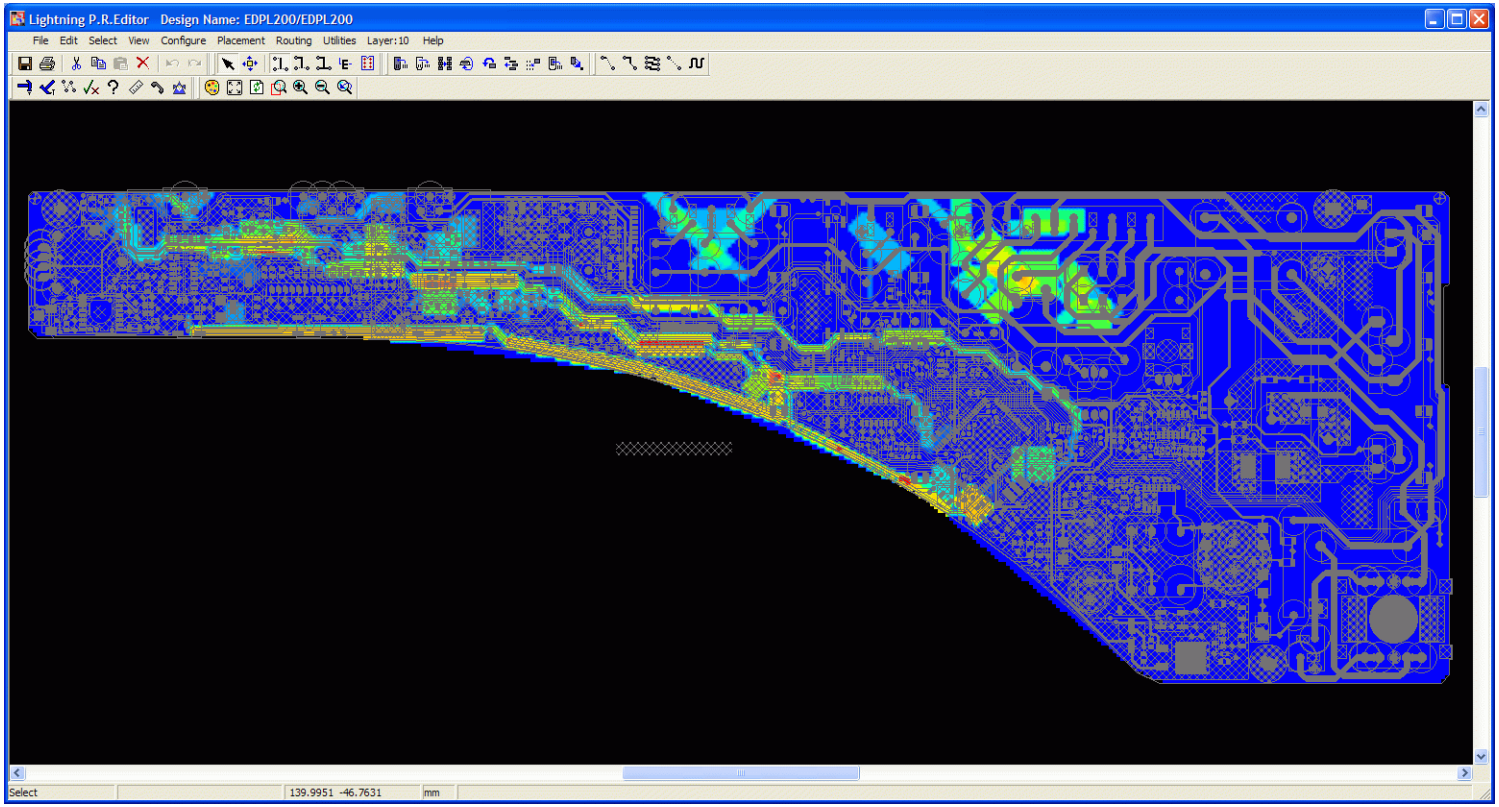
- Caused by parasitic antennas which are built up by:
  - Board to heat-sink coupling
  - Coupling between connectors
  - Board to connector coupling
  - Connector to heat-sink coupling
  - Coupling through cables





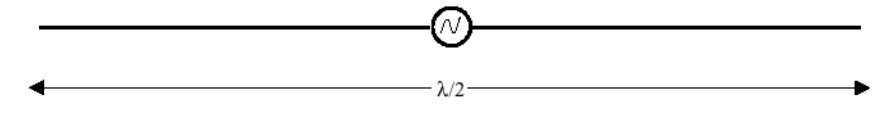
EMC-Mechanismn: Common Mode EMC

Common Mode: I/O-Coupling



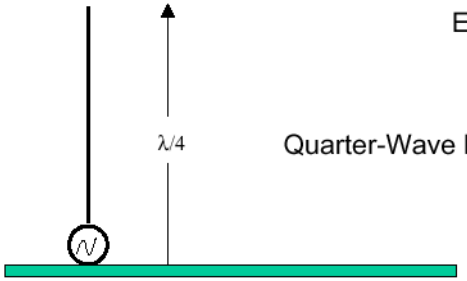
Crosstalk between fast signals to neighbourhood (IO) lines will cause noise voltages visible at the connectors

Again: Effective Antennas



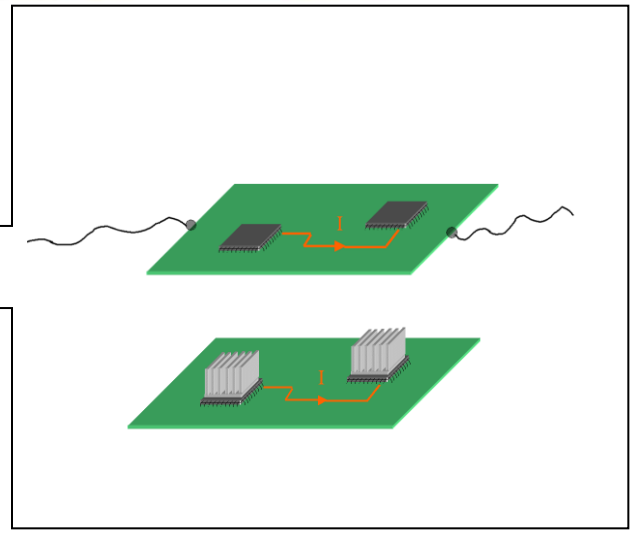
Half-Wave Dipole

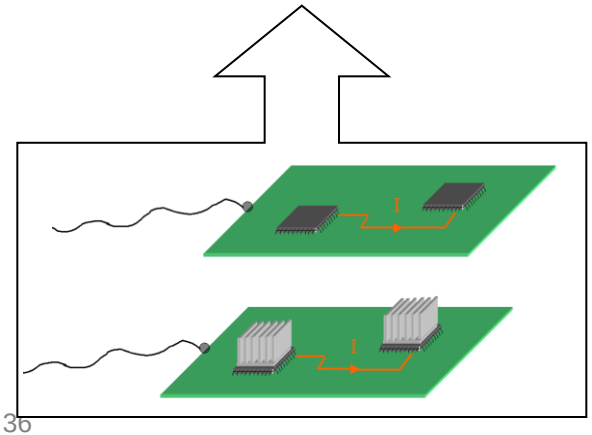
Electrically Small Loop

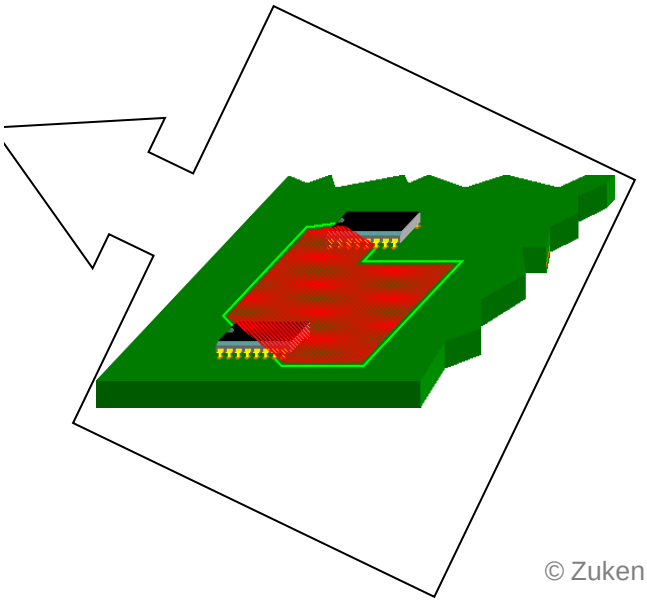


Quarter-Wave Monopole

- **Size**
- **Two Halves**





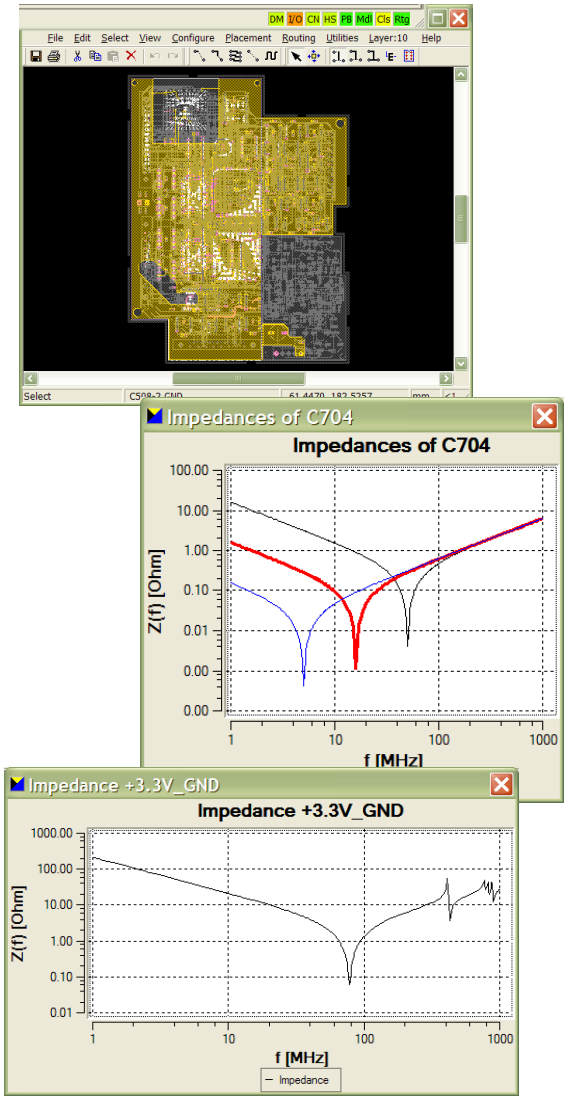


PI Advance - Power Integrity Analysis

Capabilities of the Lightning PI Advance Power Integrity Solver

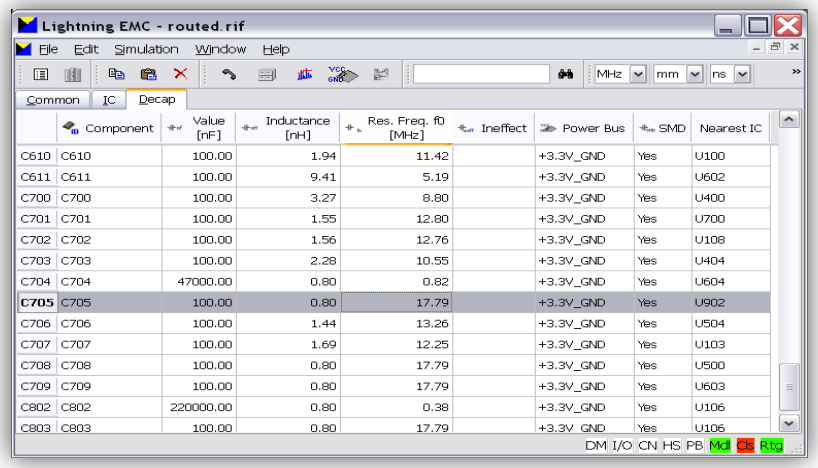
☑ Fast method to investigates the quality and efficiency of all supply systems of a PCB:

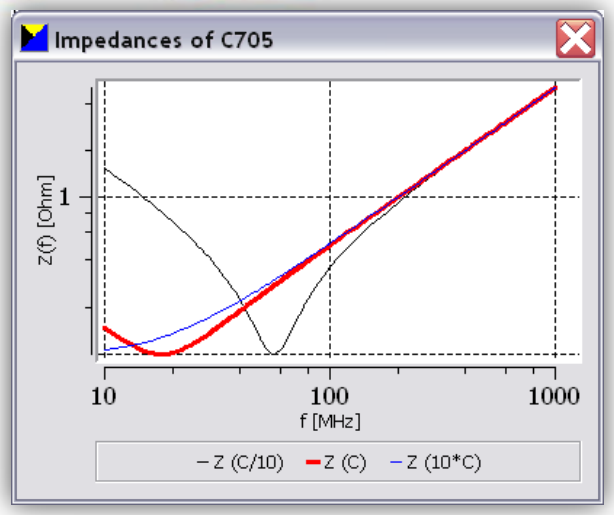
- Detection of:
  - ✓ Ineffective decaps,
  - ✓ High impedance connection of decaps to power supply system,
  - ✓ Critical input buffers, w.r.t. the power bus noise voltage.
- Estimation of:
  - ✓ Effective capacitance of total power bus,
  - ✓ Total power bus impedance (including self resonances),
  - ✓ Current drawn by each IC,
  - ✓ Power bus noise voltage, and
  - ✓ Radiated electrical field.



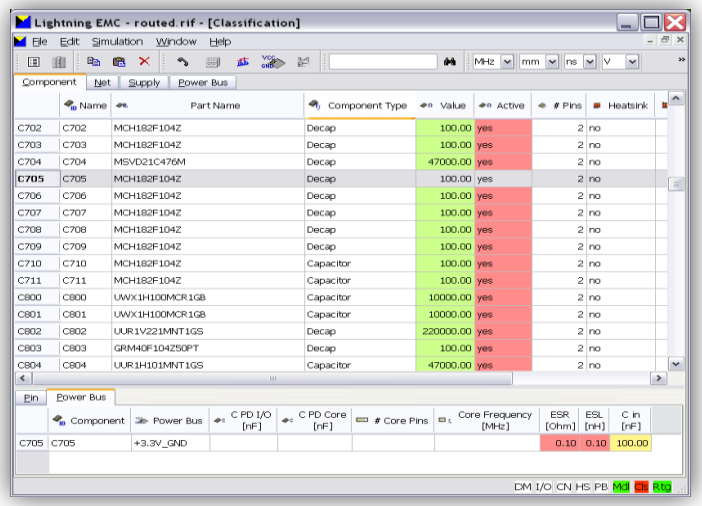
PI Advance: Decoupling Analysis & What If

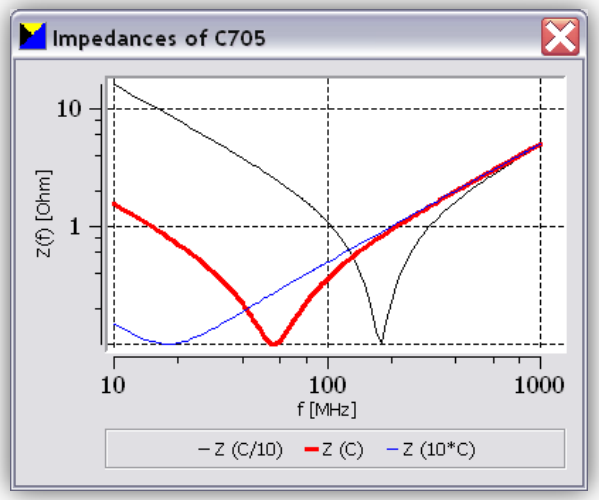
DeCap potentially not effective ?





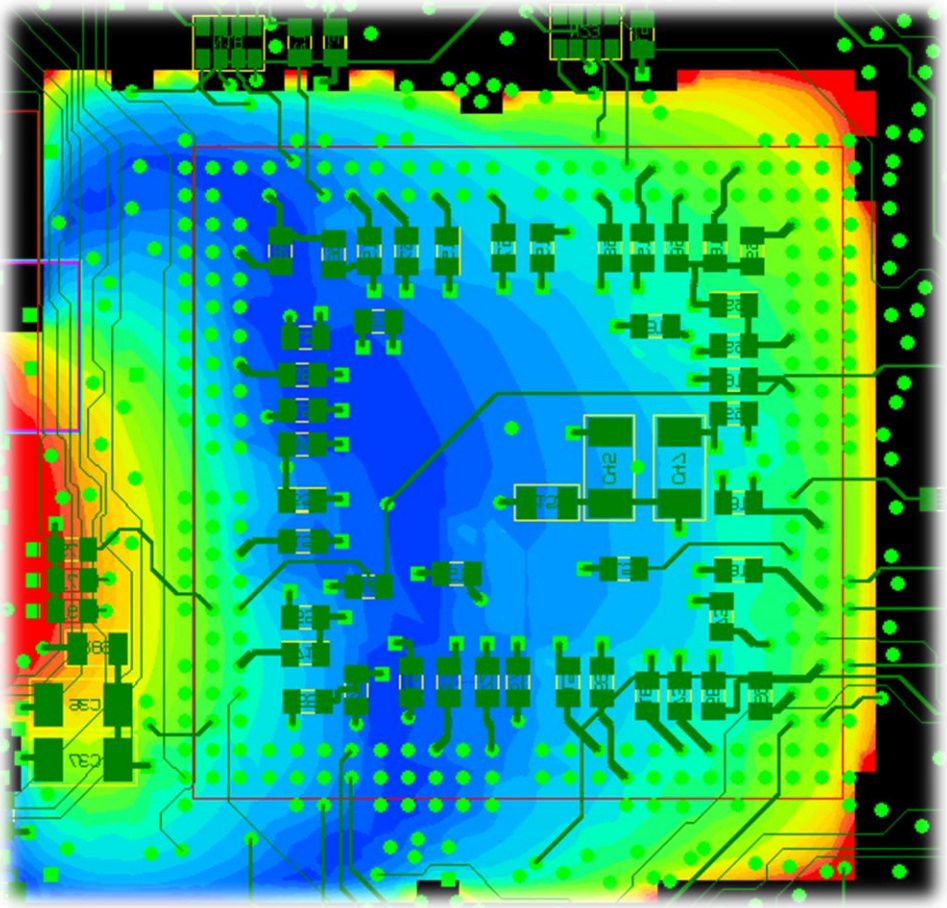
Change Value within Lightning from 470p to 100N → **Quick What-If**





PI Advance: Decoupling Effectiveness over frequency for Copper Power Areas

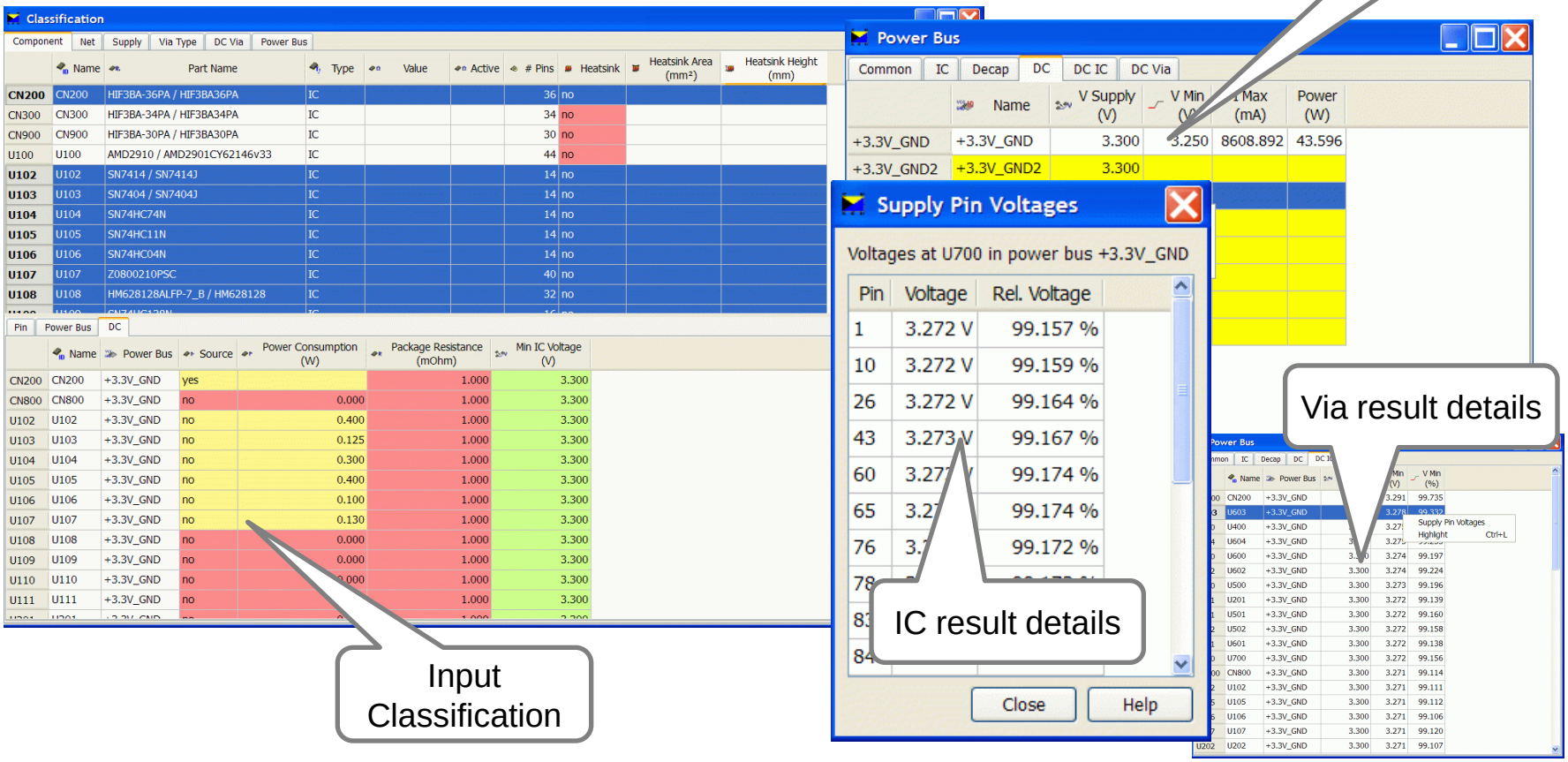
- Impedance distribution at target frequencies show impact of decoupling capacitors
- Indicate quality of placement location, value and connection inductance
- Placement or connection can be changed on the fly in P.R.Editor for what if capabilities



Lightning PIA: DC Power Integrity

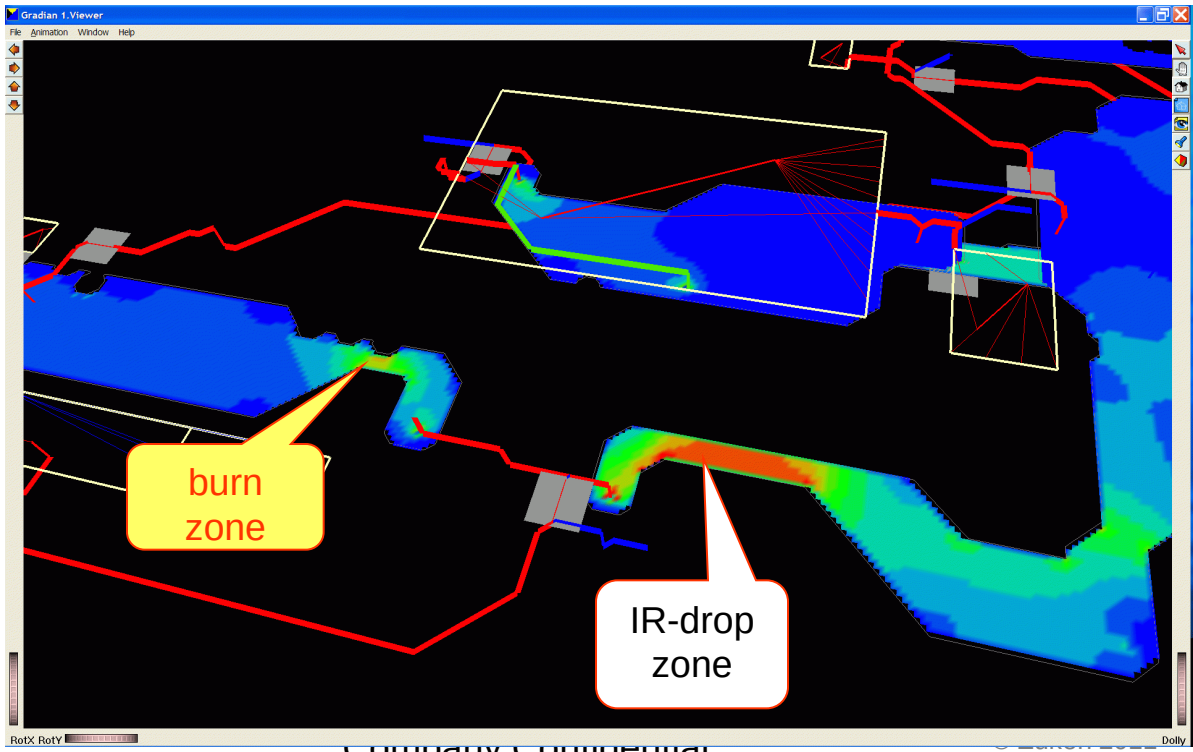
DC-Analysis of supply systems

- Table driven DC-Analysis
- Results for supply system / ICs / Vias in separate tables



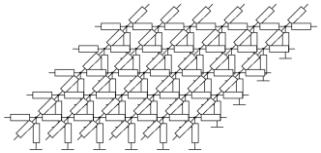
Lightning PIA: DC Analysis

- DC solver allows analysis of DC Current Distribution and IR-Voltage drops within PCB Supply nets
  - → High Current Nets as well
  - → Detection of potential trouble areas in the Layout
  - → Avoiding thermal problems and Power Supply problems

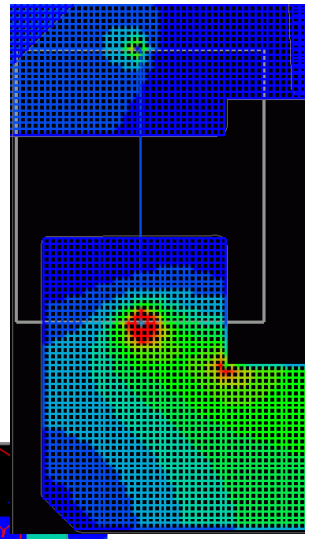


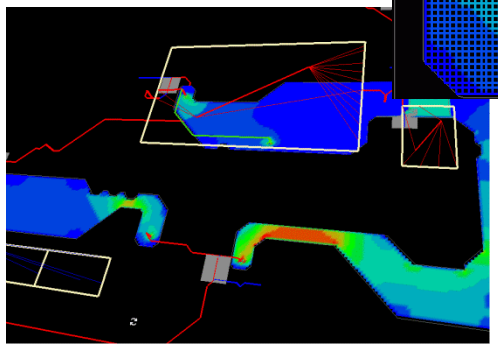
PI Advance DC Analysis

- Analysis is done highly accurate by numerical solution
  → R-Cells Grid based approach



- Analysis is done very efficiently
  → large electrical system is divided into smaller portions
- Results are visualized graphically in 3D
- Tabular results given in spreadsheet
  - Can easily be compared with given limits





Power Bus

Common | IC | Decap | DC | DC IC | DC Via

	Component	Power Bus	V Supply [V]	V_Min [V]	rel. V_Min [%]
CN501	CN501	SW+3.3V_EURO_GND_AUDIO	3.300	3.300	100.000
IC106	IC106	SW+3.3V_EURO_GND_AUDIO	3.300	3.199	96.930
IC103	IC103	SW+3.3V_EURO_GND_AUDIO	3.300	3.197	96.888
IC102	IC102	SW+3.3V_EURO_GND_AUDIO	3.300	3.197	96.885
IC104	IC104	SW+3.3V_EURO_GND_AUDIO	3.300	3.196	96.846
CN107	CN107	SW+3.3V_EURO_GND_AUDIO	3.300	3.181	96.400
CN106	CN106	SW+3.3V_EURO_GND_AUDIO	3.300	3.181	96.400
IC403	IC403	AU+11V_EURO_GND_AUDIO	11.000		
IC402	IC402	AU+11V_EURO_GND_AUDIO	11.000		

Per net and IC

IC per Pin

PowerBus/IC:

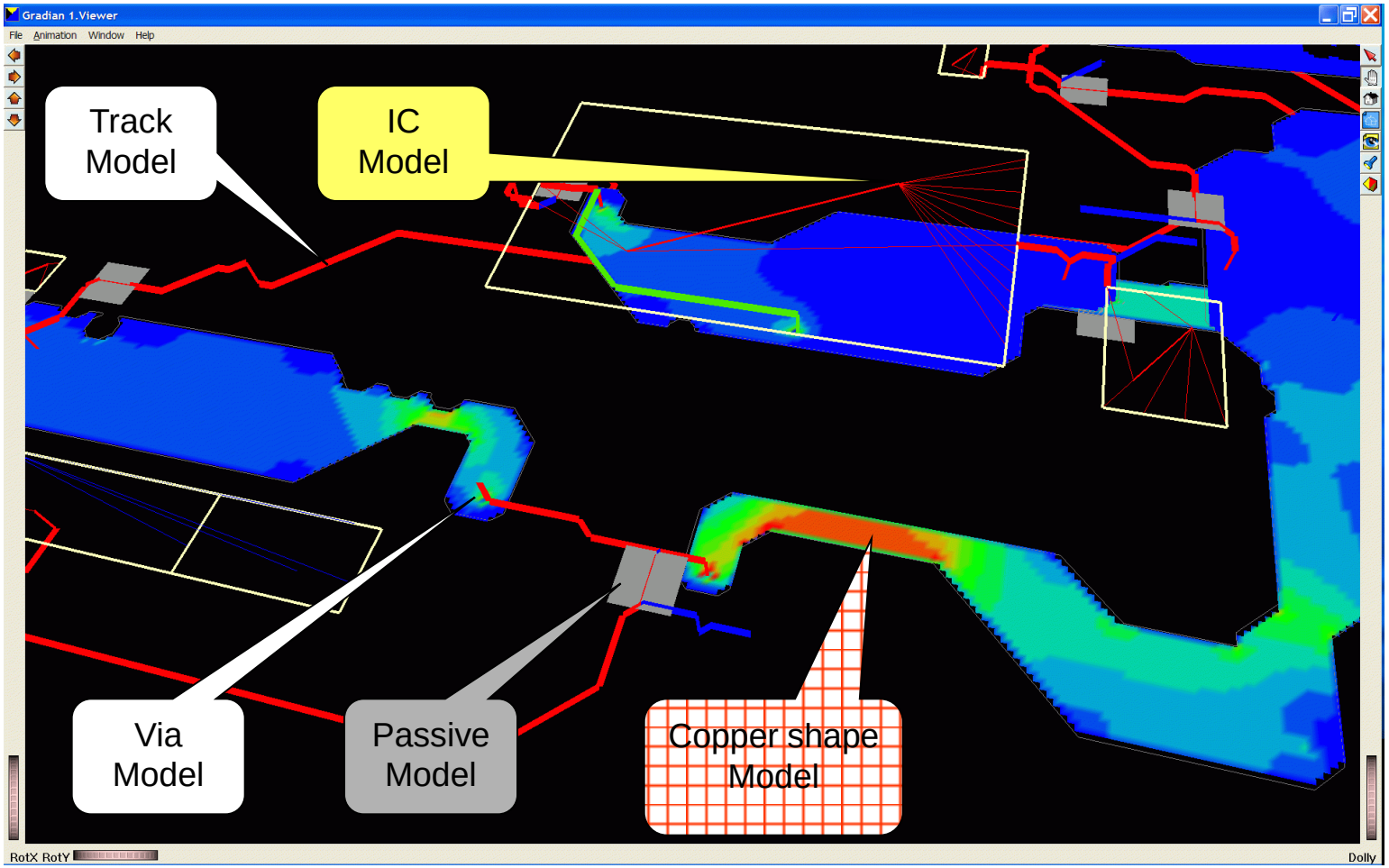
IC104 SW+3.3V_EURO_GND_AUDIO

Pin Name	DC Voltage
49	3.196 V
43	3.196 V
27	3.196 V
14	3.196 V
9	3.196 V
3	3.196 V
1	3.196 V

Per IC pin

PI Advance DC Analysis

- Model Details



Sample: Investigation of critical Power Bus

+1,8V-GND - DC Simulation

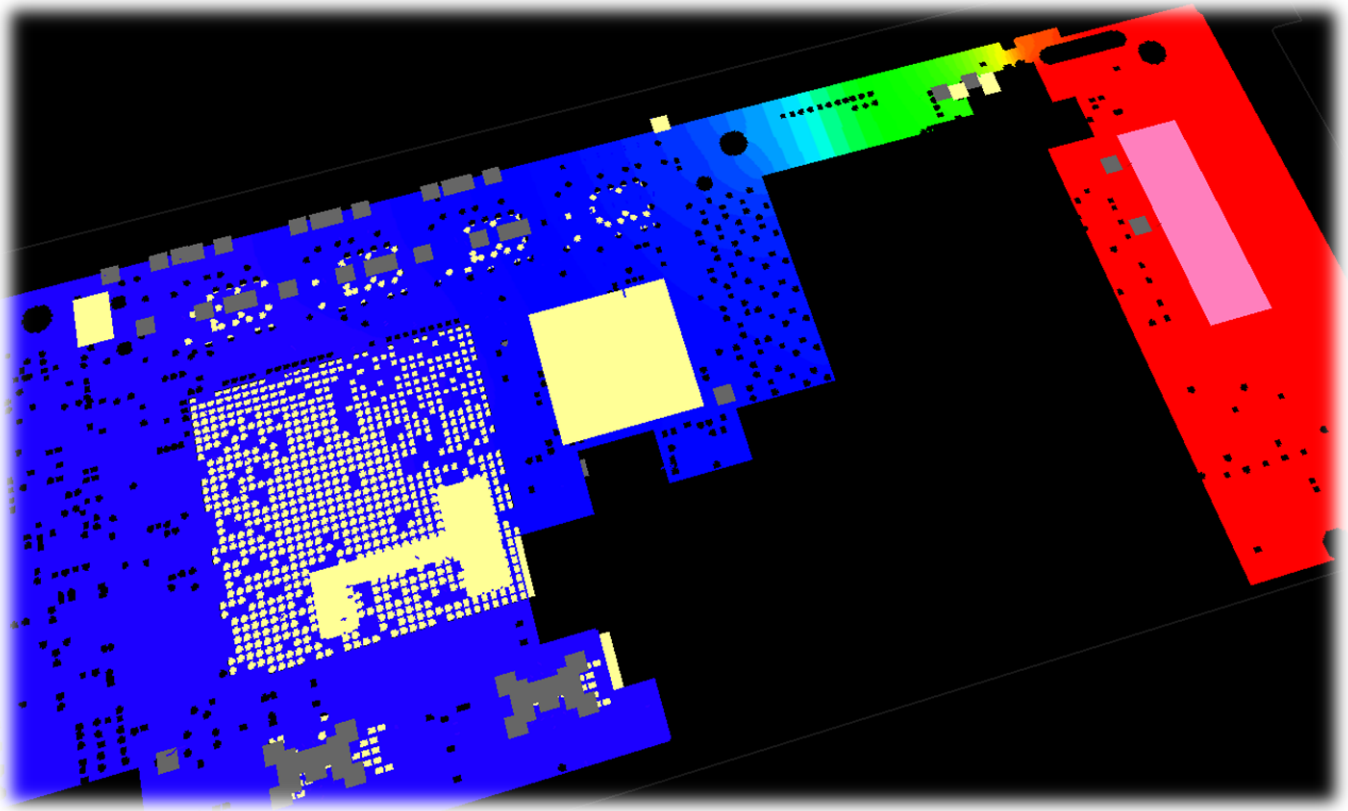
Common	IC	Decap	DC	DC IC	DC Via

	Name	V Supply (mV)	V Min (mV)	I Max (mA)	Power (W)
+1,8V_GND	+1,8V_GND	1800.00	1768.43	2183.24	3.93

Grid Size

Min Grid Size: 50.000 µm

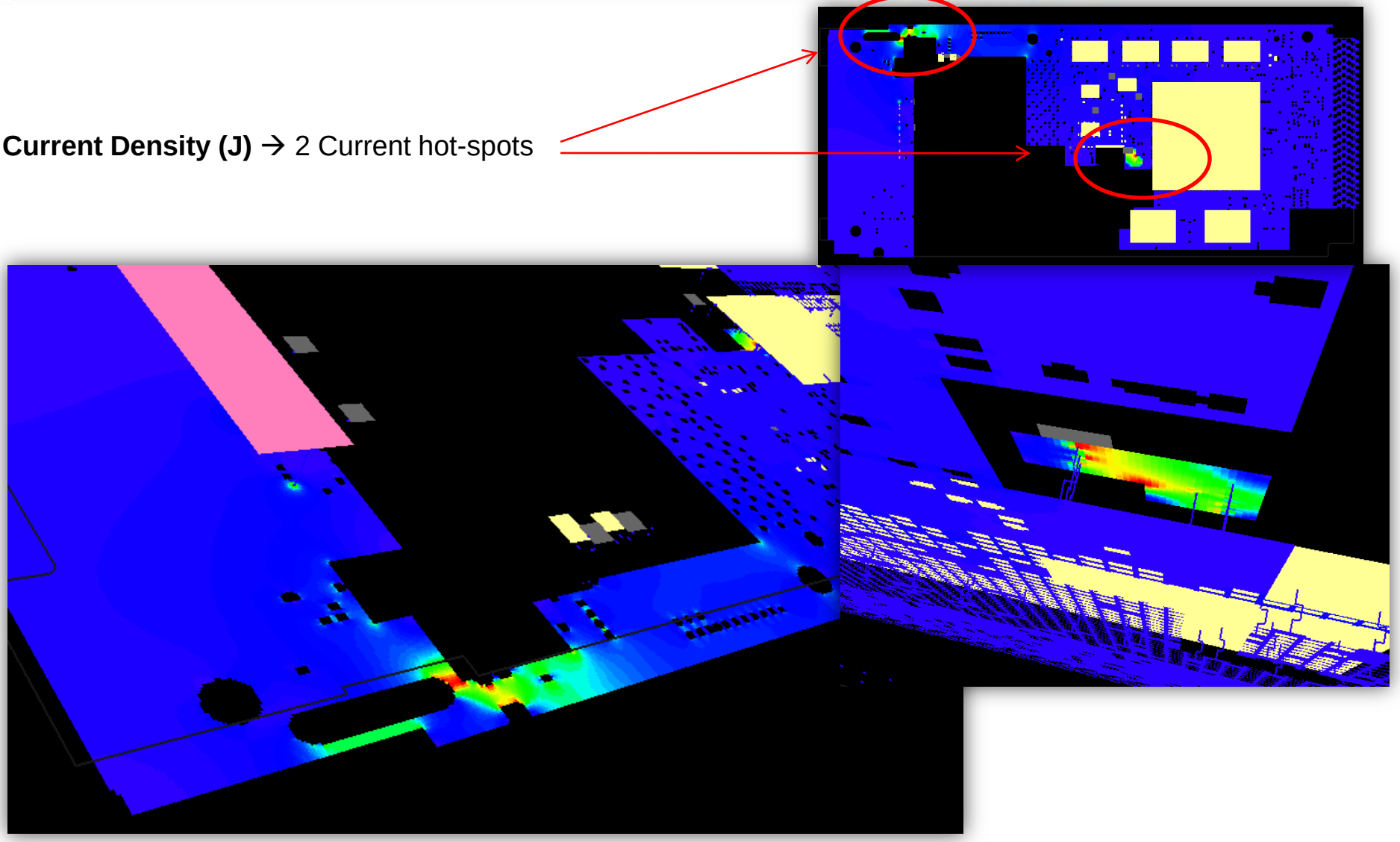
Max Grid Size: 200.000 µm



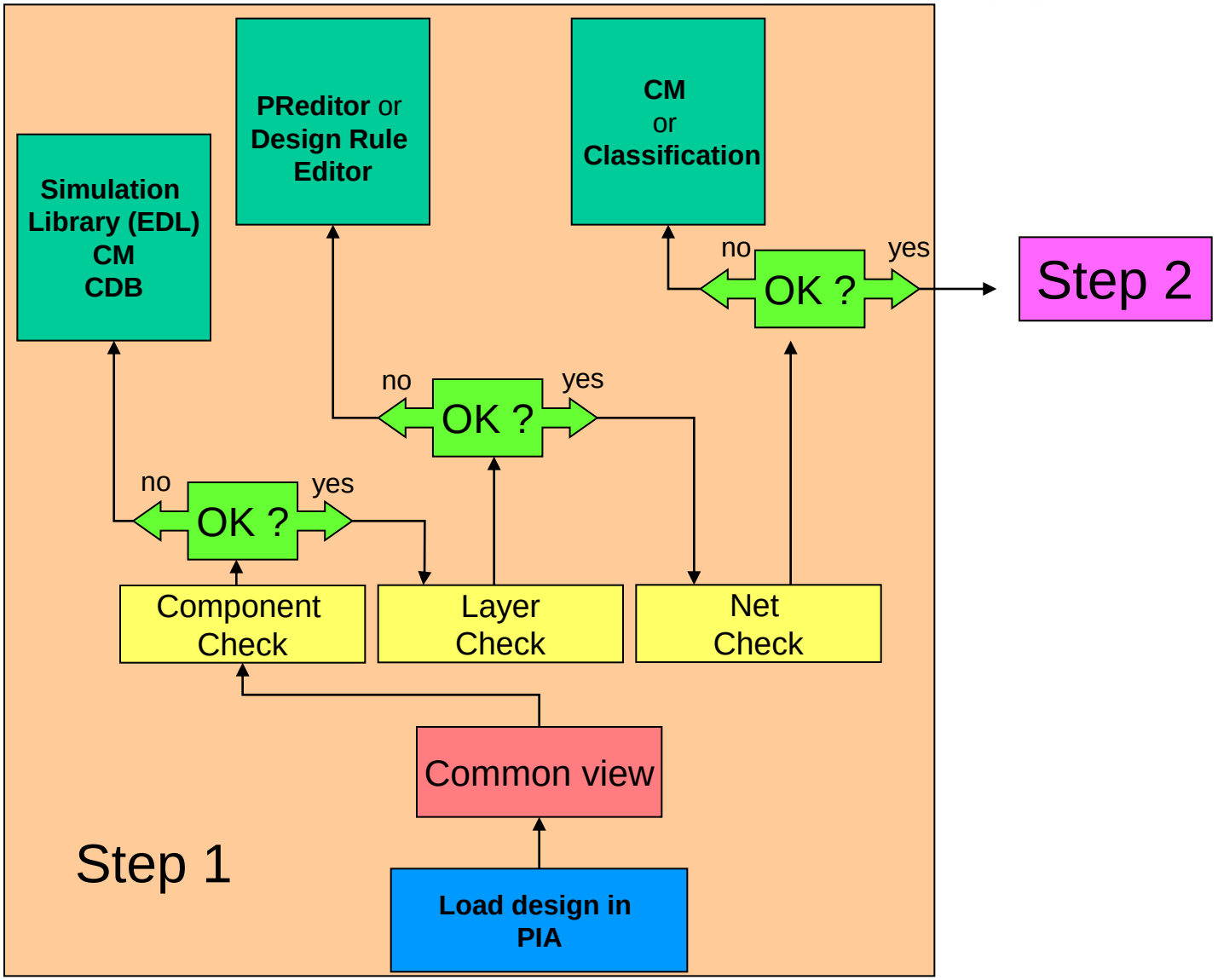
Voltage Distribution (V):
Max. Voltage Drop = 32mV

Investigation of critical Power Bus:
+1,8V-GND - DC Simulation

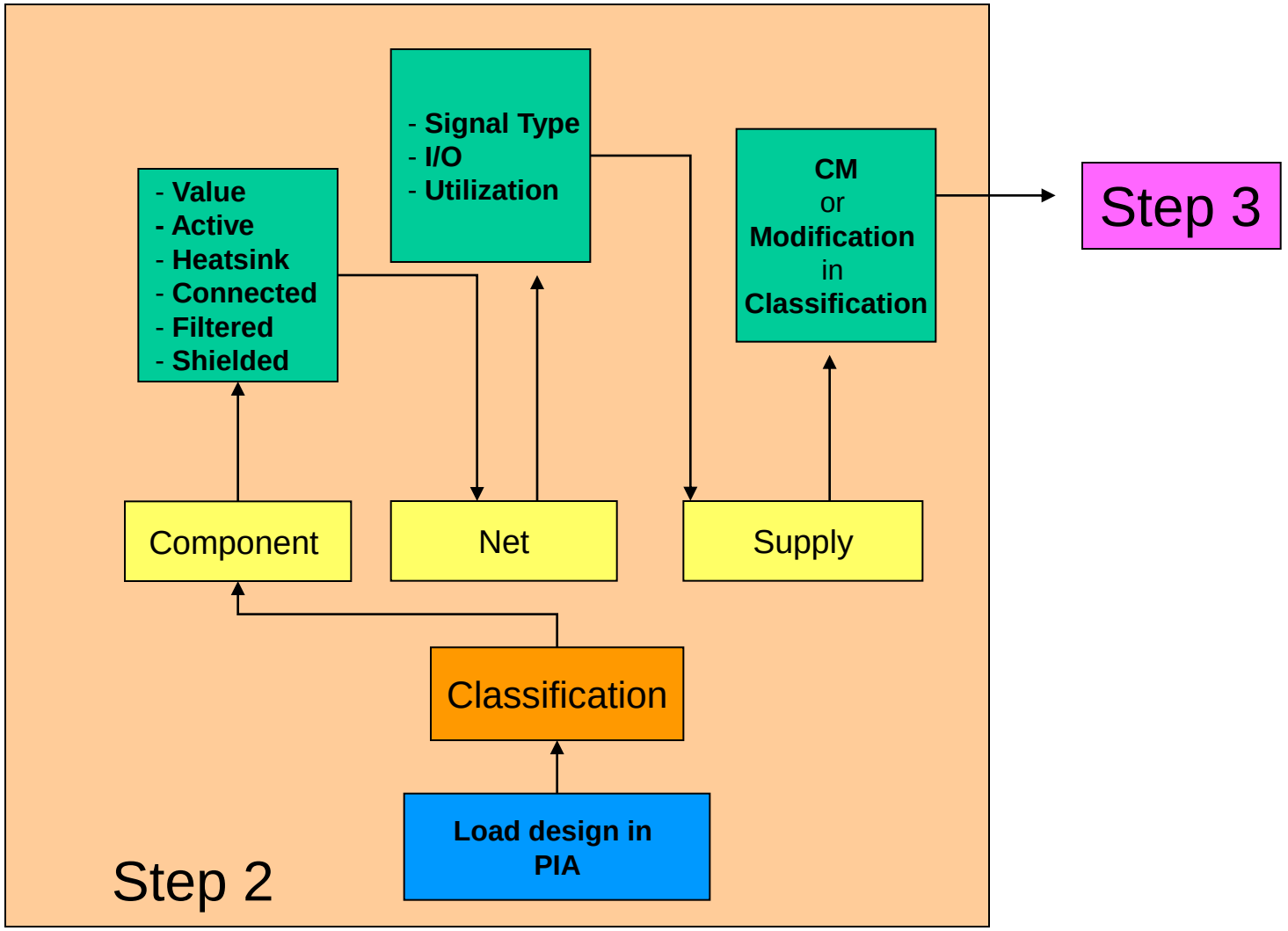
Current Density (J) → 2 Current hot-spots



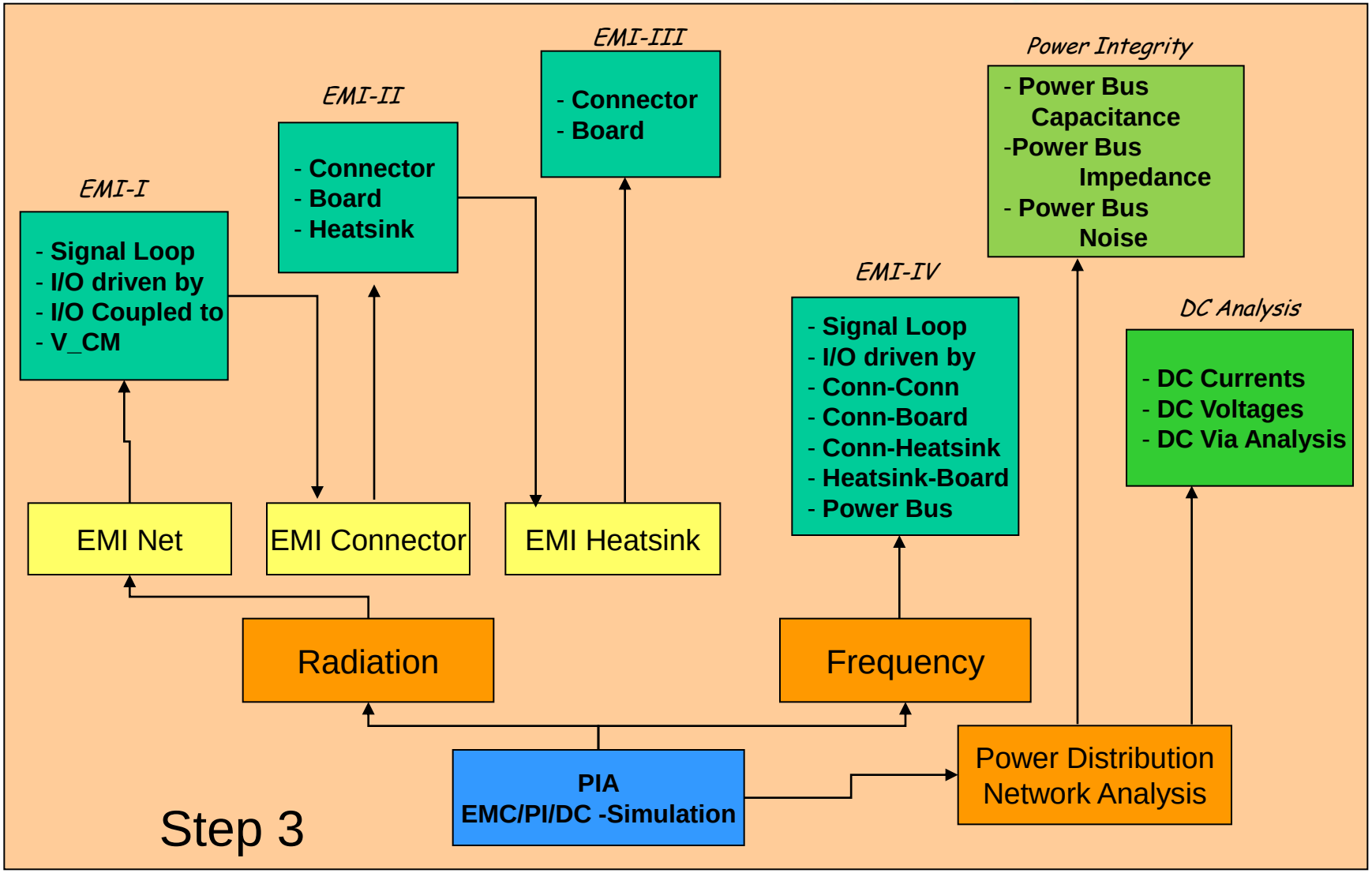
PIA Working Flow (1 of 3)



PIA Working Flow (2 of 3)



PIA Working Flow (3 of 3)



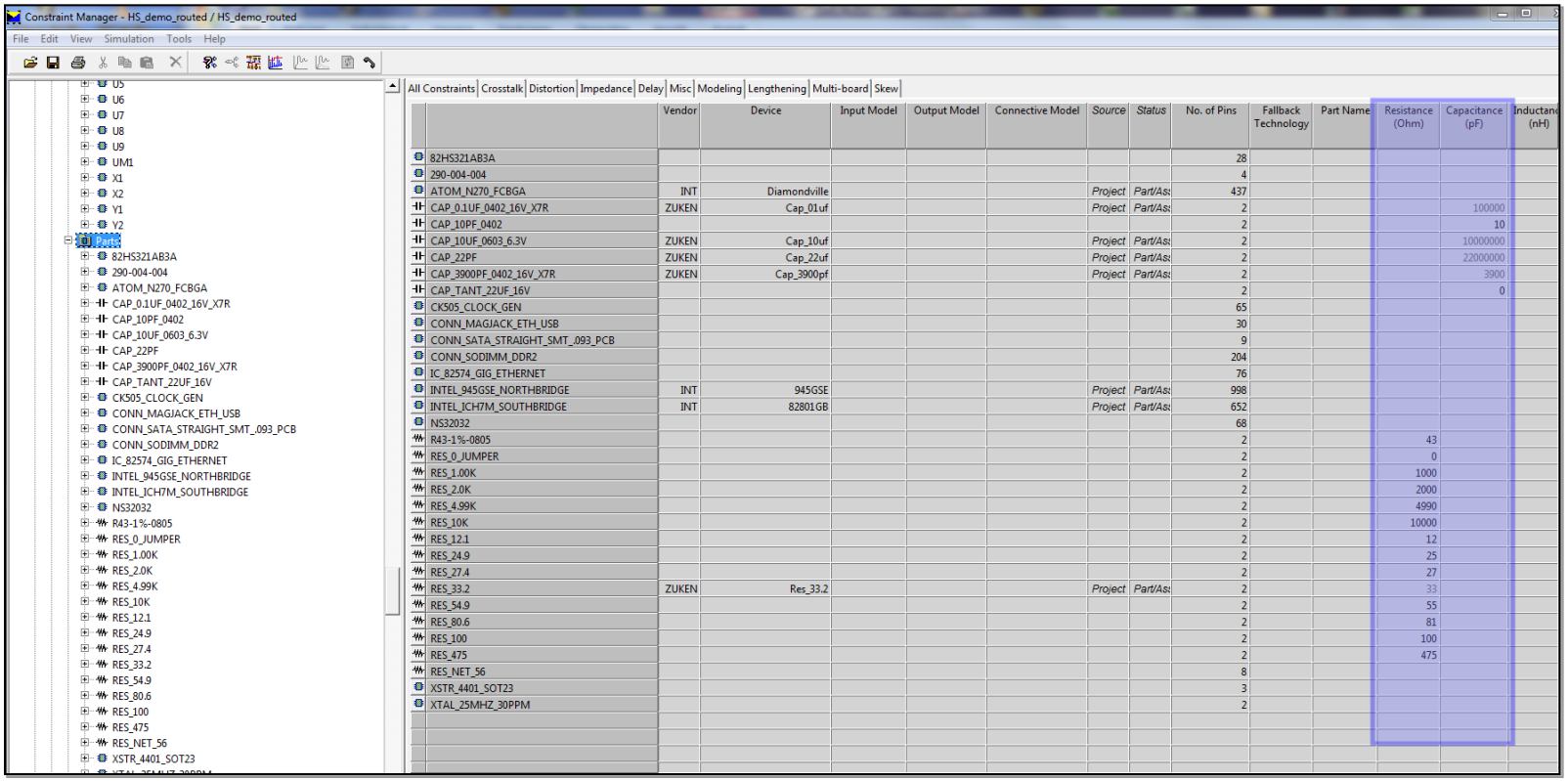
Library/Attribute Information for PIA

- PIA needs some information (of course) to work properly (but no special models nor special data setup is necessary) – even better, in a high-speed or SI flow it should work smoothly.
- It needs information (like a human expert), otherweise its blindfolded (like a human expert will be too).
- It does not need special models, but if presents uses information from IBIS models assigned
- First of all, it needs copper (airlines are not antennas, templates have no capacitance) – however, the board must NOT be completely routed !
- The user has to a certain extend interact with the software (→ Classification), this is a mandatory step !
- With respect to data, PI Advance needs to know:
  - Layer stack (not a surprise, correct ?)
  - Materials (conductivity)
  - Device types (RES/CAP/IND), as well ICs and Connectors (for EMI analysis)
  - Heatsinks (for EMC analysis)
  - Values of discrete components
  - Power/GND Pins of devices (connection to power supply systems)
  - ESL/ESR values of DeCaps (for PI AC analysis)
  - Source/Sink Current Path and Power Dissipation of ICs(for PI DC analysis)

Exercise 1: Check Design Data for PIA

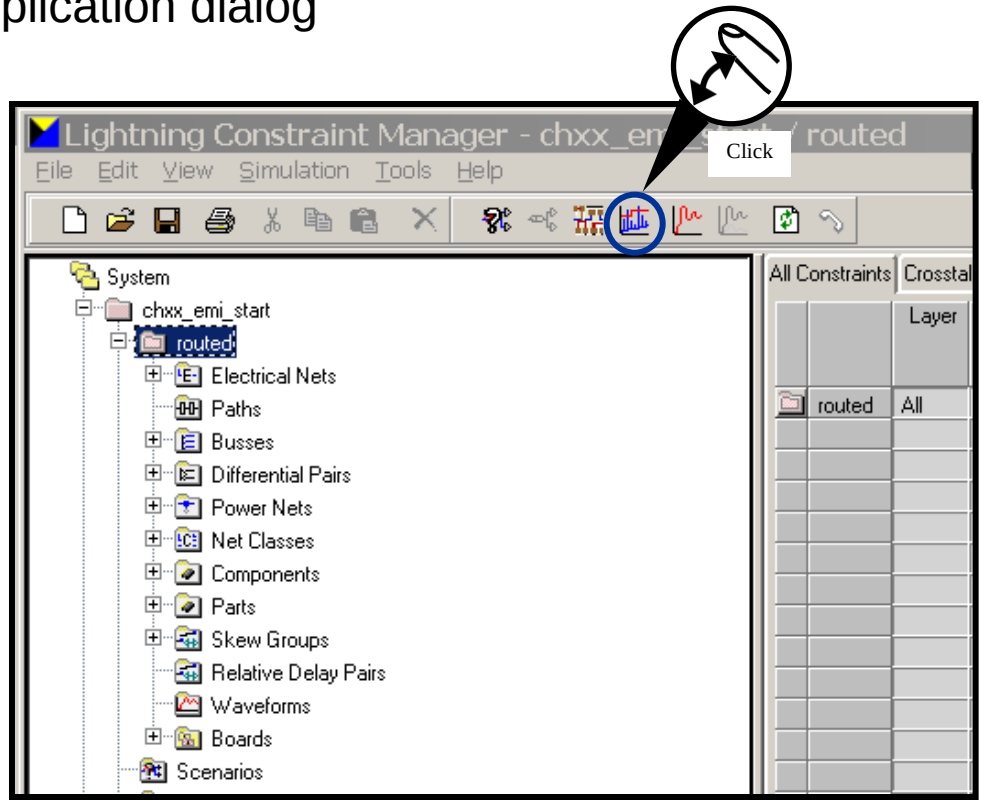
Steps:

1. Launch Pred-HS on design *hs_demo_routed*
2. Select Parts in the CM Tree View
3. Switch to Modelling TAB
4. Compare the entries with those in the picture, **discuss** differences and impact of those (ICs but as well resistors and capacitors) **with your trainer**.(we will fix that later in an exercise and with provided data set)



How to launch PI-Advance

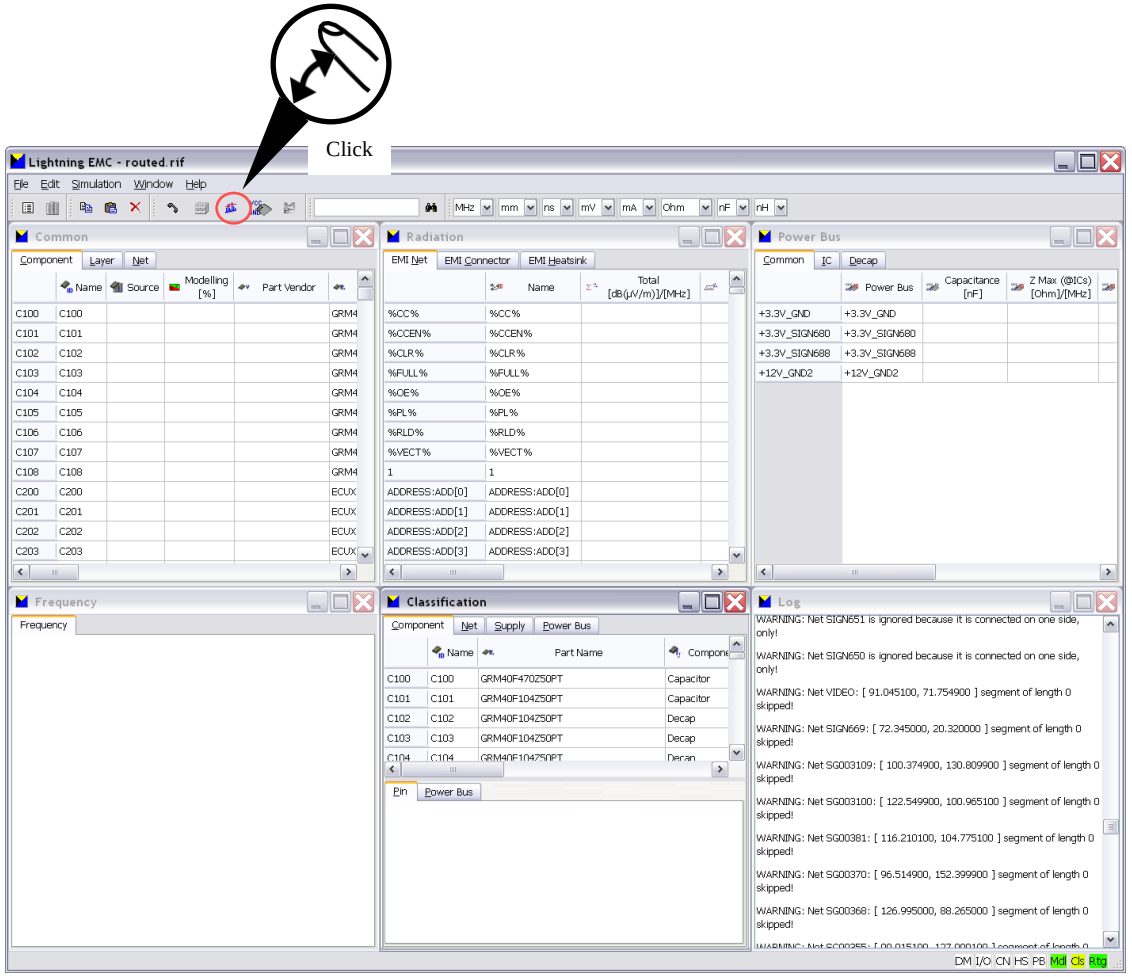
- From the software bundling point of view PIA is an add-on option to PReditor HS (mandatory), but not license wise related to SI-Verify
- PI-Advance is to be launched from CM using the  icon (or Tools-PIA)
- PIA Icon gets active (only) when a license is present !
- PIA will start up as separate application dialog



Exercise 2: Launch PIA & perform a EMI Analysis

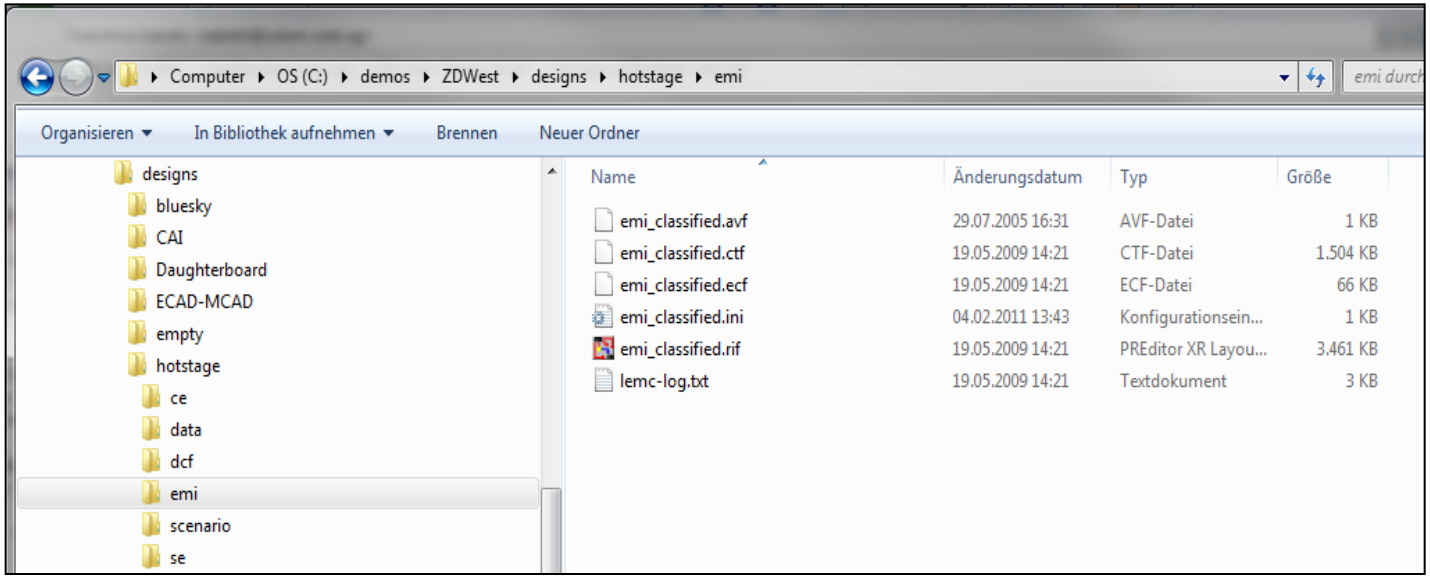
Steps:

1. Launch PI Advance on design *hs_demo_routed*
2. Run EMC Analysis 
3. Raise Result Window (Radiation)
4. Inspect the various GUI columns
5. Why some columns in the various results window are empty, others are filled ?

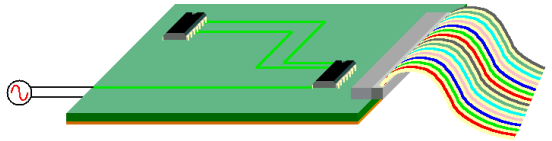


PI-Advance Information: Data Files

- Some technical details behind
  - PI Advance reads **CTF** and **RIF** files from <design>\hotstage\emi directory
  - As PI Advance needs the newest RIF format , PI Advance keeps a clone of the design RIF and CTF under <design>\hotstage\emi directory
    - Stored as well is classification data (.ecf) and options (.INI)
    - These files are stored in XML or plain ASCII



PI-Advance Information:
SI-Simulation vs. PIA EMC Analysis

	SI-Simulation (LT/SIV)	PI Advance (EMC)
Function	Considers the Signal Quality (Signal Integrity) . Means the quality of signals which arrive at the receiver. (Reflection, Crosstalk, Timing).	Analyses the various Radiation effects on PCBs. → Which enets could be responsible (in worst case) for radiation.
Typical model	Driver-TL-Receiver 	Driver-TL-Receiver-current + current return path (+ IO-Lines + connectors) → System 
Results	Very accurate. The simulation results can be compared against measurement.	It shows where the problems are (could be). The results are not matchable (comparable) to the results from the measurement (chamber) but…

PI-Advance Information:
SI-Simulation vs. PIA EMC Analysis

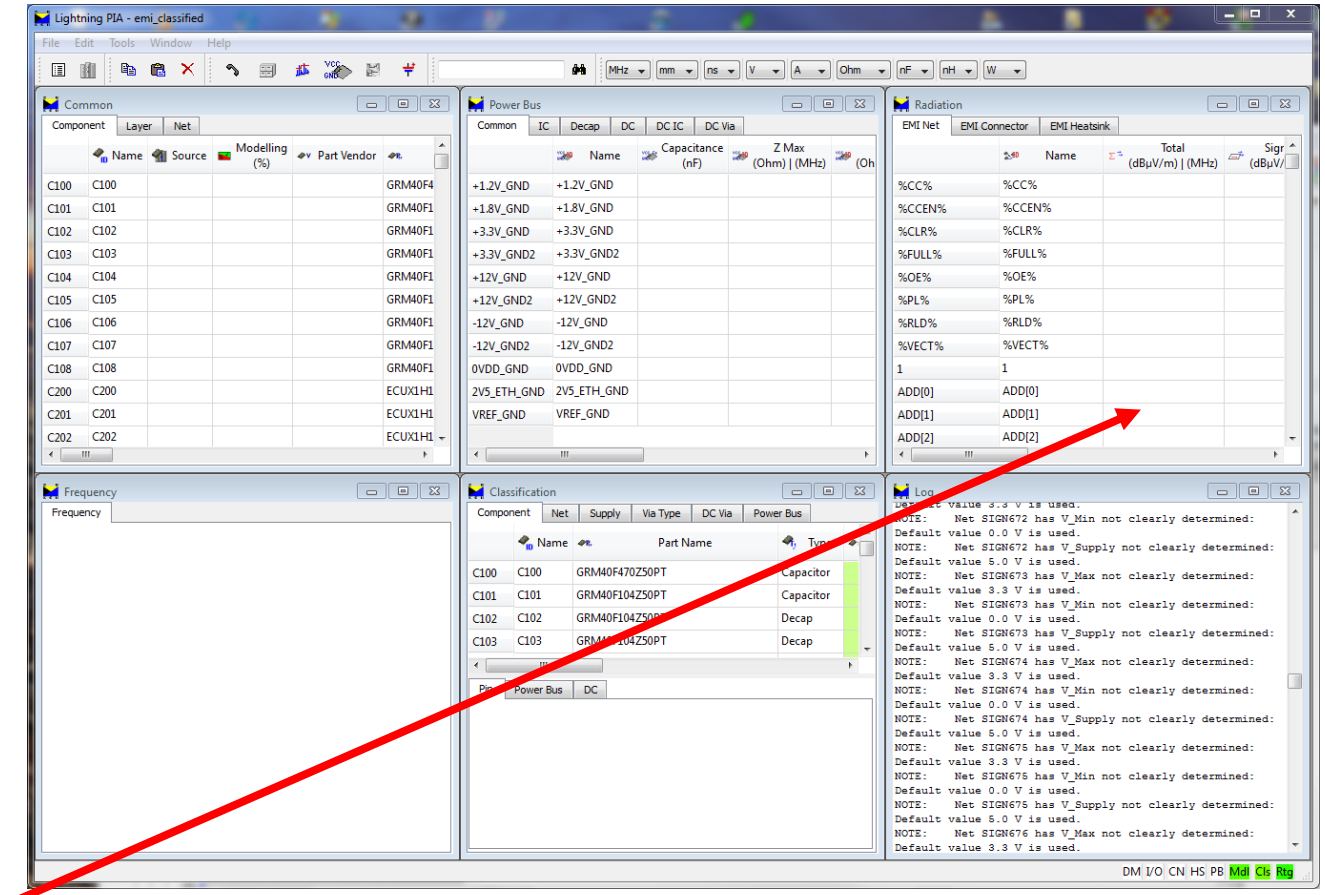
	SI-Simulation (LT/SIV)	PI Advance (EMC)
Process (relevant for simulation)	scs.exe (interactive simulation) scs.exe (batch simulator) impulse.exe (Library) Client Server architecture, if needed, SCS will restart automatically	engineer.exe engineer_solver.exe Only 1 engineer can run properly on a system. (On hang-up, user may have to restart the system (because new bmsmain process is needed → sweeper)) Needs/uses impulse.exe as well !
Required data	CTF	RIF + CTF, to be found in the directory: <design>\hotstage\emi Classification file .ECF
Results are computed by	Field Solver + Simulation Engine (Telegrapher Equation Solver) Time Domain !	Fast UMR (University of Missouri Rolla) EMC algorithms for full PCB EMC simulation, developed by UMR EMC Expert System consortium. Frequency Domain !

PI Advance GUI

When PI Advance is launched (after CM has written the design data), the GUI is populated with the current design data

→Some pre-processing is done on these data

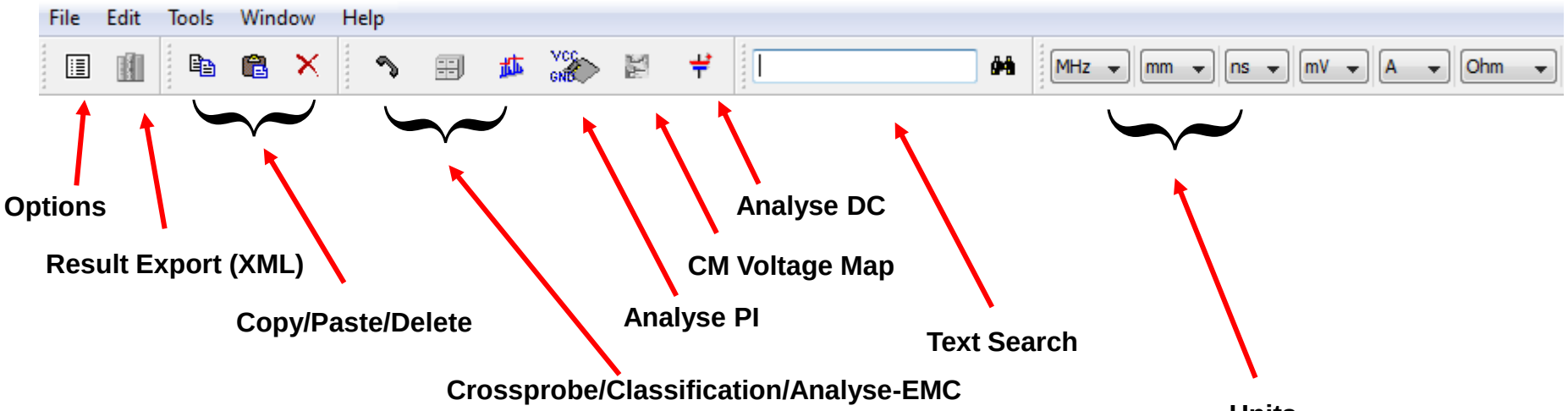
→ Only Common (and classification if data is there) cells are filled.



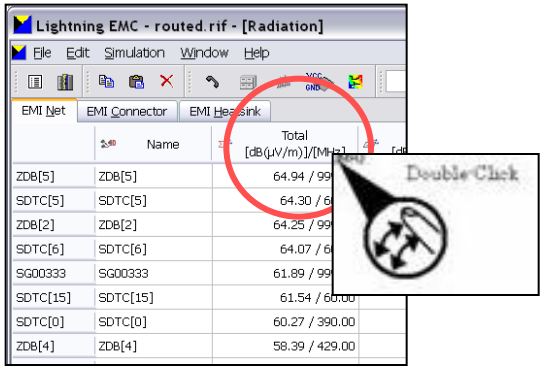
There are no results available then !

PI Advance GUI Issues (1 of 5)

- Top Menu+Icon Bar



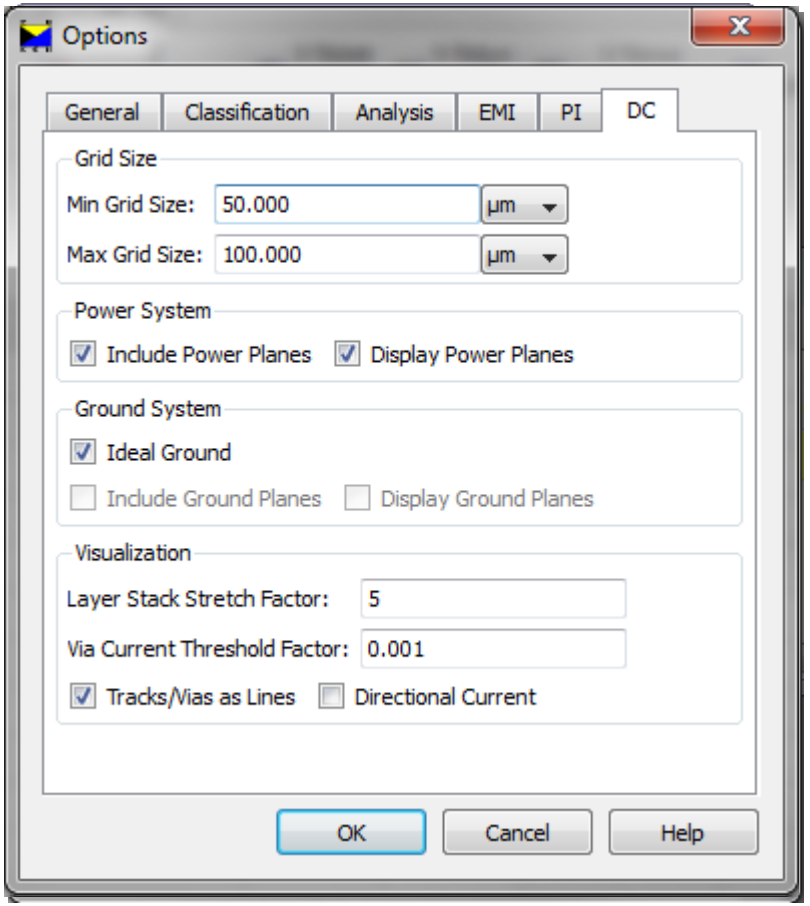
- Analysis Icon:
  - **Sensitive** if no results are there, **insensitive** after analysis
  - Becomes sensitive again if settings or data have changed (results are discarted then)
- All columns can be sorted (click on column header):
  - Ascending
  - Descending



PI Advance GUI Issues (2 of 5)

Options:

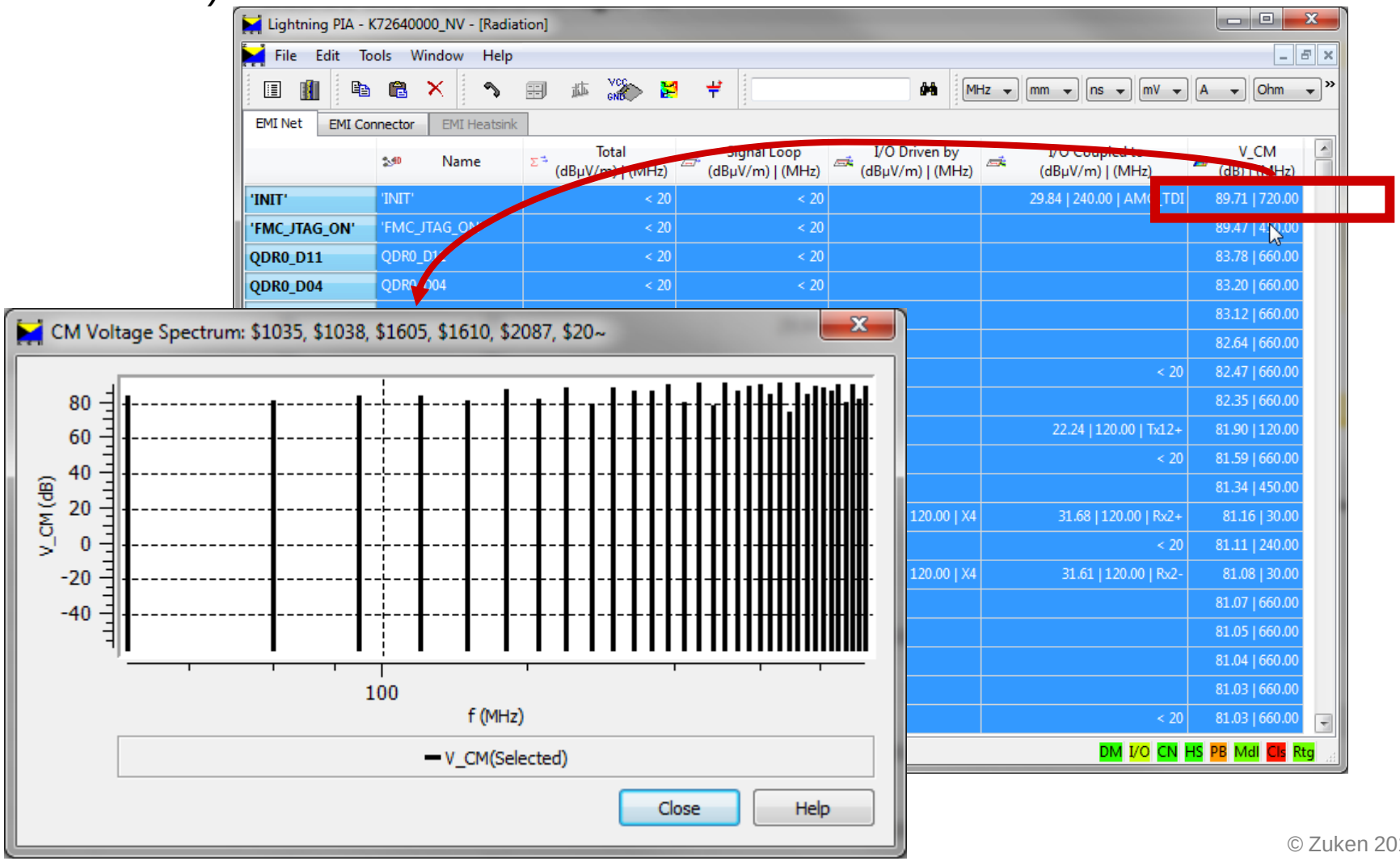
- General: Decimal points & axis control
- Classification
- Analysis Settings
- EMI: Change antenna distance for far field analysis (>= 3m)
- PI: Effective Series Resistance (ESR) and Effective Series Inductance (ESL) defaults, analysis settings (RLC grid size and grid size relaxation level)
- DC: Grid Size settings, Power/Ground system settings and visualization issues



PI Advance GUI Issues (3 of 5)

Additional information in most table cells (double click of right mouse button RMB)

RMB



PI Advance GUI Issues (4 of 5)

Status Bar (lower right of PI-Advance):

The first 5 indicators show green, yellow, or red levels of emissions for a specific EMC effect. These change their status when a given, user-definable threshold is passed. The thresholds are given in dB(µV/m).

- **DM:** Differential mode emission
- **I/O:** Emission due to I/O-coupling
- **CN:** Cables, attached at connectors act as antenna for current driven common mode emission.
- **HS:** Heatsinks, act as antenna for current driven common mode emission.
- **PB:** PowerBus noise caused emissions.

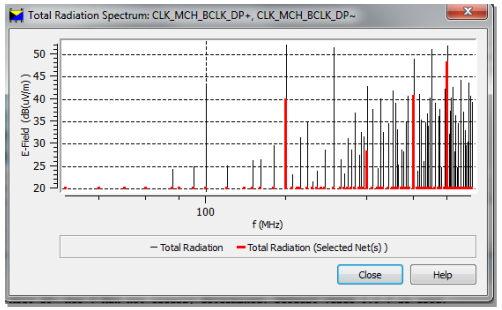
The last three indicators have a continuous color between red and green depending on the percentage of:

- **Mdl:** I/O buffer models available at IC pins
- **Cls:** Classification settings are not set to default for: Net type, Clock frequency, Rise- and Fall times
- **Rtg:** Routing completion of the non-supply nets.

PI Advance GUI Issues (5 of 5)

Result/Plot Windows (Spectrum, Impedances)

All spectral results can be visualized graphically by pressing the right mouse button (RMB) on a selected result cell of a frequency domain result. Spectral plots resp. impedance plots are available for the following result types:



- Electric field strength
- Impedance of the power bus and DeCaps
- Noise voltage due to switching currents
- Common mode voltage due to the signal current per E-net.

Zooming

- Within these plot windows you can always **zoom in** by opening a rectangle with the left mouse button pressed. Using the middle mouse button, the zoom area returns to the previous state.

Scaling

- The type of scaling (linear or logarithmic) and the displayed ranges can be controlled individually for the x- and y-axis within the **Option Dialog**, depending on the content of the plot. The frequency axis will always be displayed in the same manner, hence the setting for this axis can be done within the General Tab of the Options Dialog.

Units

- The units can be changed within the Options Dialog, General Tab or within the toolbar, if this is enabled in the Options Dialog.

Time for a break...